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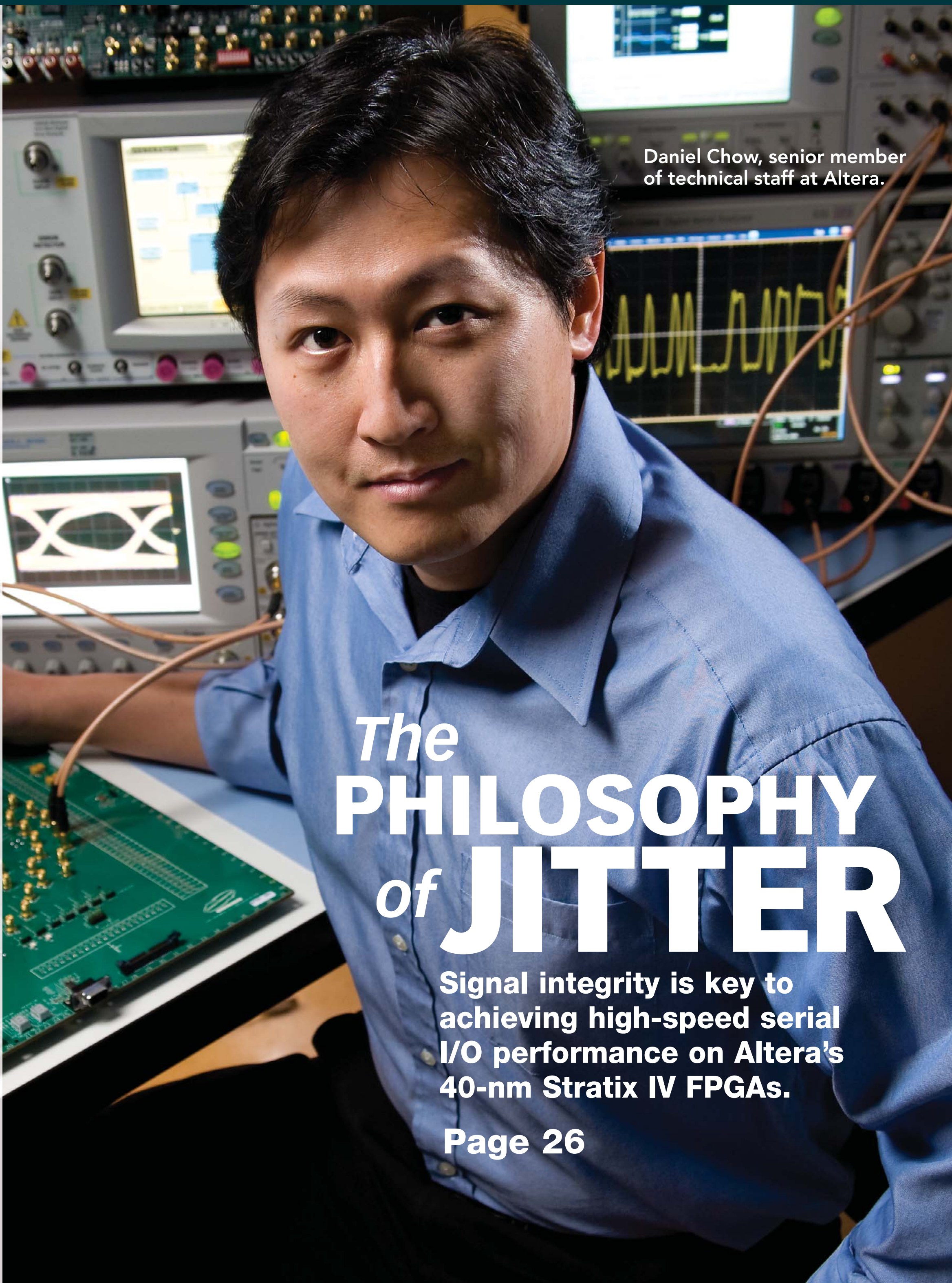
Test & MEASUREMENT WORLD

THE MAGAZINE FOR QUALITY IN ELECTRONICS



Daniel Chow, senior member of technical staff at Altera.

The PHILOSOPHY of JITTER

Signal integrity is key to achieving high-speed serial I/O performance on Altera's 40-nm Stratix IV FPGAs.

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Tabor's New WS8101/2 Arbitrary/Function Generators

The Wave Standard Series is a family of single and dual channel arbitrary / function generators, designed to provide superior performance at a low price. The new series incorporates Tabor's award-winning "best of both worlds" technology, having both memory-based, true arbitrary waveform generator architecture for accurate, jitter-free waveforms alongside a DDS-based generator to create all the standard modulation formats. Packed into a compact and efficient 2U -rack size box, all in one easy-to-use high performance unit, makes the Wave Standard series, by far, the best in its category (AFGs) for size, price and performance.

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MODEL	Tabor WS8101/2	Agilent 33250a	Tek AFG3102/2
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Architecture	True Arb + DDS	DDS Only	DDS Only
Max Frequency (Sine/Square/others)	100MHz | 100MHz | 12.5MHz	80MHz | 80MHz | 1MHz	100MHz | 50MHz | 1MHz
Max. Sample Clock	250MS/s	200MS/s	250MS/s | 1GS/s
Max. Memory Size	512k	64k	16k to 128k | 2 to 16k
Vertical Resolution	16 bits	12 bits	14 bits
Max Amplitude (into 50W)	16Vp-p	10Vp-p	10Vp-p
Rise / Fall Time	< 5ns	< 8ns	< 5ns
Square Wave Jitter (rms), typ.	< 100ps	< 100ps	< 200ps
DC Levels (into 50Ω)	-8V to +8V	-5V to +5V	-5V to +5V
Modulation	AM, FM, FSK, PSK, Sweep	AM, FM, FSK, Sweep	AM, FM, PM, FSK, PWM, Sweep
Connectivity	LAN, USB, GPIB	RS232, GPIB	LAN, USB, GPIB
Warranty	3 years standard	1 years standard	3 years standard
Strating from Price	$3,750 | $4,950	$4,571	$3,760 | $4,960

Specification compiled from Tabor 8101/2 data sheet, Agilent 33250a data sheet 5968-8807EN, March 14, 2005 and Tektronix AFG3000 data sheet 76W-18656-3, 12 November 2007. Prices are taken from the vendors websites.

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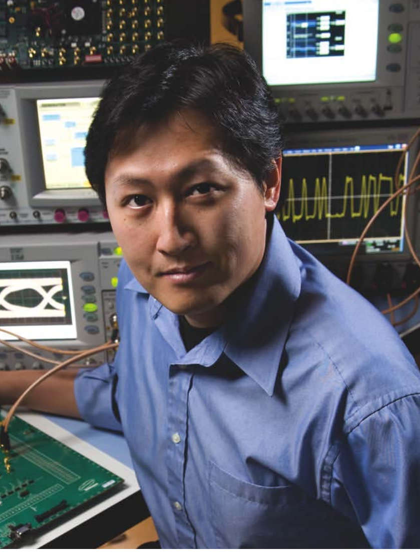

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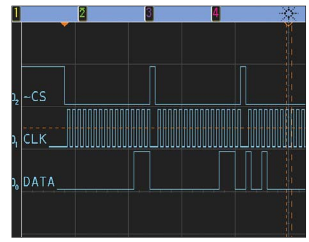

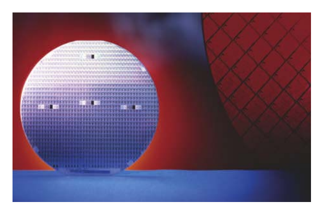

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Power technologies to be "amplified" at IMS2009

Power amplifiers continue to be one of the hot topics of 2009, according to Fred Schindler, general chair of this year's International Microwave Symposium (IMS), scheduled for June 7 to 12 in Boston, MA. "The mobile Internet is driving 4G and even 3G mobile devices. . . with ever-higher bit rates, and we can't afford to drain the battery very fast," said Schindler. "That's why there's such a push into amplified technologies." Schindler discussed this year's IMS in a phone interview.

www.tmworld.com/ims2009_interview

Blog commentaries and links

Taking the Measure

Rick Nelson, Editor in Chief

- "Just in time" to prevent a recovery?
- Innovation catches curveball illusion
- Avoiding solar disaster
- Mildly impressed by MiFi

Rowe's and Columns

Martin Rowe, Senior Technical Editor

- IEEE issues call for help
- Software and soldering irons
- It's the inductance that matters

Engineering Education and Careers

Jennifer Kempe, Contributing Editor

- Research in recovery
- Robotics on the rise

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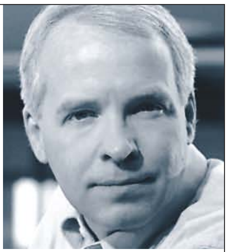
EDITOR IN CHIEF



Will electronic ink save print?

Will devices like the Kindle revive the fortunes of "print" publications? Amazon and newspapers hope so, according to "Amazon Hopes Its Bigger Kindle Ignites Demand," posted May 7 on the *Wall Street Journal*'s Website. The article notes, "As part of the efforts to broaden the Kindle's appeal, the publishers of the *Washington Post, New York Times,* and *Boston Globe* will test selling the Kindle DX at a reduced rate to a small number of people that subscribe to their Kindle editions."

Magazines, too, are getting into the Kindle business; 29 magazines (including, oddly, the online-only magazines *Salon* and *Slate*) are available for Kindle on amazon.com as I write this. Print magazines offering Kindle subscriptions include mostly news and literary titles (for example, *Time* and *The New Yorker*); the tech community is represented only by *MIT Technology Review*—and, if you like, a couple of science-fiction titles.

Print will survive because it cuts through the online noise.

So, will Kindle catch on as the new medium for traditional print magazines and newspapers? Writing in the "Brian's Brain" blog at edn.com, Brian Dipert is skeptical. He writes, "At 2.5x the total screen area of the Kindle 2 (9.7" diagonal versus 6"), it's got the hardware chops to render large-format newspapers in a reasonably readable manner. But its $489 price tag (plus media subscriptions!) isn't amenable to mass adoption, especially in this dismal economy."

I'm with Brian. The Kindles (both the smaller Kindle 2 and new bigger DX) seem extremely expensive for what they do (download, store, and display static black-and-white content). For the price of a Kindle, you could almost get a laptop or a couple of netbooks. Furthermore, we've heard a lot about convergence, but Kindle and other readers seem to take a step in the wrong direction—creating yet another electronic device to drag along.

I'm not convinced that even free electronic devices can offer a reprieve for troubled newspapers. Writing April 3 in the *Huffington Post,* the author and journalist Will Bunch advocated "Giving Away Free Netbooks to Save America's Newsrooms." He writes, "Big-city newspapers...should have teams of people walking up and down the rowhouse streets of a city like Philly, giving these newfangled devices away to people who've been left behind by the Computer Age, and perhaps also offering them at reduced prices to people who can afford them and simply want easier or more convenient online access."

That sounds reasonable, and even feasible if netbook prices fall below $100, as has been predicted by Jen-Hsun Huang, the chief executive of Nvidia. And I'm sure there are some people left behind by the computer age who would like to take advantage of such an offer. But many people have been left behind by the computer age because they want to be left behind—or perhaps they have caught up with the computer age at work but want to leave it behind when they get home. You could give these people a $2500 MacBook Air and they won't read the *Boston Globe* or the *New York Times* or the *Washington Post* on it. And finally, when the dust settles, print—ink on paper—is going to survive because, whether or not you've been left behind by the computer age, it's going to be the medium that cuts through the online noise. T&MW

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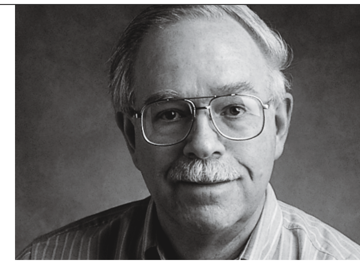

Arts and crafts for test

Living in an area that isn't exactly a hotbed of electronics technology, I acquire most components from mail-order sources. Two Radio Shack stores located within 13 miles offer limited (to put it mildly) parts inventories.

Needing a thin, sharply pointed test probe with a long reach, I assembled one from a length of hollow plastic rod, some heat-shrinkable tubing, and a long needle. To obtain the needle, I visited an arts and crafts store. In addition to a plethora of needles in all sizes, I found a variety of materials that might prove useful in the test lab. Note that the engineering characteristics of these materials may vary from source to source.

DANIEL GUIDERA

For example, the craft-supply store offers a range of foamed plastic shapes that can serve as insulation for heat-sensitive circuits, as non-RF-absorbent structural supports for EMI tests, for oddities such as large foam-cored toroidal inductors, and possibly as conical antennas. The consistency of foamed plastic varies, and closed-cell formulations offer more rigidity than open-cell and water-absorbent foams used for supporting live flowers.

Paper-coated foam board comes in handy for assembling structural prototypes and for the layout of a discrete-component printed-circuit board. Glue a 1:1 copy of the component-outline drawing to the board and "stuff" the drawing with through-hole components. Note that foam-core board may prove hazardous to components that are sensitive to electrostatic discharge, so use a sacrificial set of parts.

A local hobby-supply store usually features a selection of metal and plastic structural shapes that includes music wire, tubing, angles and strips, and sheets. You may be familiar with the "gimmick"—two lengths of wire twisted to form a crude capacitor of a few picofarads. As a more formal alternative, you can cut a length of small-gauge brass tubing and slip it over a length of insulated hookup wire. Using AWG #18 PTFE-insulated hookup wire and tubing just large enough to accommodate the wire, I measured approximately 3.2 pF per inch of tubing. Adding a length of heat-shrinkable tubing completes the "capacitor." The same brass tubing can also shield a wire or form the outer conductor of custom-made coaxial cable.

Some call electronic testing an art, but it's also a craft. T&MW

GET CRAFTY

Browsing through a craft or hobby store can be almost as much fun as shopping in a well-stocked electronics surplus outlet. I visited the West Lebanon, NH, branch of Jo-Ann's Fabric and Craft Stores, of Hudson, OH (www.joann.com). Independently owned Valley Art Suppliers (also located in West Lebanon) sells modeling supplies, kits, hand tools, and small hardware. In both stores, I noted a few products that may solve odd problems in the test lab or prototyping shop:

Materials:

Dow Chemical manufactures Styrofoam materials and shapes that are available under various resellers' brand names (craft.dow.com/craft/about/index.htm).

K&S Engineering's point-of-sale displays feature music wire, structural metals, and plastics (www.ksmetals.com).

National Balsa produces balsa, hardwood, and lightweight plywood stock in various thicknesses and dimensions (www.nationalbalsa.com).

Darice makes glass and other beads (component standoffs) and copper wire in nonstandard colors (www.darice.com).

Adhesives:

Adhesive Technologies offers hot-melt and conventional adhesives for industrial and craft applications (www.adhesivetech.com).

Loctite Division of Henkel supplies cyanoacrylate ("super glue") and other adhesives for the consumer and hobby markets (www.loctiteproducts.com).

Duncan Enterprises manufactures Aleene's and other brand names of general-purpose and specialized craft adhesives, including fabric-specific glues (www.duncancrafts.com).

Small tools:

Jewelry and crafting tools include wire cutters, pliers and crimpers, a wood-burning pencil that could double as a soldering iron, and an embossing tool that's a small hot-air gun.


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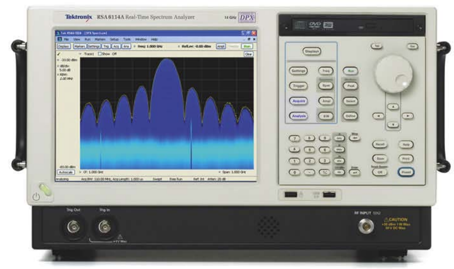
Agilent 34970A switch/measure unit
Agilent 34980A switch/measure unit

Tektronix enhances swept-spectrum analysis



Tektronix has announced enhancements for its RSA6000 Series spectrum analyzers. The instruments, which incorporate the company's DPX technology, offer combinations of time- and frequency-domain measurement capabilities that make them suited for spectrum-management, radar, electronic-warfare, and radio-communications applications, said Darren McCarthy, RF technical marketing manager at Tektronix.

The enhanced instruments address the issues raised by the prevalence of digital RF technology, added McCarthy. The combination of digital computing with gigahertz RF frequencies and multi-radio environments, he said, has introduced new analysis challenges, making it necessary to measure broadband transients, root out digital-signal-processing errors, and identify so-called runt pulses.

An improved broad sweep capability in the RSA6000 Series spectrum analyzer allows quick detection of signals of interest, with the DPX engine now able to collect hundreds of thousands of spectrum sweeps per second over a 110-MHz bandwidth. Users can sweep the DPX across the full input range of the RSA6000, up to 14 GHz, reducing the chance of missing time-interleaved and transient signals during broadband searches.

With the new "Trigger on This" feature, users can select a signal of interest merely by pointing at a signal on the analyzer's display. Other enhancements include the new runt trigger function and the ability to time-qualify any trigger, all of which, McCarthy said, will enable users to find the one pulse in a thousand that doesn't meet spec. The base price of the enhanced unit is $77,900, and user-installable upgrade packages for existing RSA6000 Series instruments are available. www.tektronix.com.

NI releases FPGA learning tool

National Instruments has unveiled what it calls a "digital learning device" that should give high school, university, and vocational students experience with digital logic and FPGA (field programmable gate array) technology. The NI Digital Electronics FPGA Board, which integrates with the NI Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) II and NI ELVIS II+ educational design and prototyping platforms, combines analog and digital design instruction in a single platform.

The centerpiece of the FPGA board is a Xilinx Spartan-3E FPGA, which can be programmed using either NI LabView or the free Xilinx ISE Web-Pack software. Students using the FPGA board can learn circuit concepts by using the NI Multisim circuit design and SPICE simulation platform. And because it is integrated with the NI ELVIS II platforms, the system offers a range of instruments—including a func-

Editors' CHOICE

Diode reverse-recovery-time tester

The AVR-CD1-B is a GPIB- and RS232-equipped instrument intended for reverse-recovery-time testing of diodes and other semiconductor devices. The AVR-CD1-B applies a 2-μs-wide forward bias pulse of +0.1 A to +10 A to a device under test. At the end of that pulse, the current ramps downward at an adjustable rate of 100 to 200 A/μs until the diode stops conducting. The current waveforms generated by this instrument are suitable for testing in accordance with MIL STD-750 E Method 4031.4 Test Condition D. Standard and customized jigs for different device packages are available.

Standard AVR-CD1-B models include one diode test jig, which connects to the instrument mainframe over a DB-25 control cable. The standard test jig contains a variety of pin sockets and posts and will accept TO-220AC (2-lead) packages and most axial packages, if the leads are bent. The jig will also accept a variety of specialized daughterboards. The output signal is provided via a BNC connector on the test jig, supporting connection to a user-supplied high-bandwidth (≥300 MHz) oscilloscope.

Base price: $18,998. *Avtech Electrosystems, www.avtechpulse.com.*

CALENDAR

Semicon West, July 14–16, San Francisco, CA. *SEMI, www.semiconwest.org.*

Design Automation Conference, July 26–31, San Francisco, CA. *IEEE, ACM, EDA Consortium, www.dac.com.*

EMC Symposium, August 17–21, Austin, TX. *IEEE EMC Society, www.emc2009.org*

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tion generator, a digital multimeter, and a 100-Msamples/s oscilloscope—that students can use to gain experience in building test benches.

NI says the board has been slated for adoption by PLTW (Project Lead The Way), a not-for-profit educational program that aims to help middle and high school students develop a strong foundation in science and engineering topics. "The new logic board based on NI ELVIS will change the way students learn digital logic design at the high school level," said Tom White, director of technology at PLTW, in a prepared statement. "More than 500 schools use our materials, and we're thrilled that, with this new product, the many students who learn lower-level introduction to logic now can make quick, natural progress to high-level languages like LabView, which makes learning fun."

"We are excited to collaborate with NI on this project," said Patrick Lysaght, senior director of the Xilinx University Program at Xilinx. "Students can learn everything from the basics of electronics all the way to advanced FPGA design with this one affordable board that combines digital logic and circuit design in one unified environment." www.ni.com.

Editors' CHOICE

Create test patterns for serial data

Receivers and transmission lines that carry serial data streams need bit patterns when tested. Two high-speed pattern generators from Picosecond Pulse Labs, the Model 12050 (12.5 GHz) and the Model 12040 (8 GHz), produce PRBS (pseudorandom bit sequence) and user-defined bit patterns that let you test the physical layer in a backplane, cable, connector, or receiver.

The instruments support PRBS patterns of 2^7–1, 2^{23}–1, and 2^{31}–1 bit lengths. You can create your own patterns up to 512 bits in length using each instrument's front panel or through its USB interface.

Signal amplitudes are programmable as well. Single-ended (50-Ω output impedance) output voltages range from 250 mV to 2 V and differential (100-Ω output impedance) signal amplitudes range from 500 mV to 4 V. You can adjust the crossing point, where rising and falling edges cross when viewed as an eye diagram, from 35% to 65% of signal amplitude. The instruments also provide trigger pulses at the start of each PRBS or user-defined pattern, which you can use to trigger an oscilloscope or bit-error-rate tester. Typical rise times are 20 ps (10% to 90%) and 14 ps (20% to 80%). You can program or adjust the output signal's DC offset from –2.5 V to +3 V.

Base price: $25,945. *Picosecond Pulse Labs, www.picosecond.com.*

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Networks work in distributed systems

When you need to keep analog measurement wires short, yet your PC is located farther away from your measurement instrument than either USB or GPIB can reach, Ethernet may just fill the bill.

Data-acquisition applications that use Ethernet include jet-engine testing, machine monitoring, oven and freezer monitoring, and power monitoring. "Power monitoring is becoming more popular with concern over energy savings," said Charlie Stiernberg, product manager for remote data-acquisition products at National Instruments.

Networked data-acquisition systems often handle high channel counts. "Typical applications for our networked data-acquisition systems use 40 to 80 channels," said Sean Sullivan, VP of engineering at Data Translation. "Applications include monitoring industrial batch ovens and battery testing where long sensor wires are impractical."

Neil Fenichel, president of Microstar Laboratories, has also seen high channel counts used in conjunction with Ethernet-based instrumentation. He cited a test system for missiles that uses 40 temperature and 40 accelerometer channels where the measurement system is 1000 ft from a control room.

Distributed data-acquisition systems needn't be that far from a PC to use Ethernet, though. Steve Radecky, product marketing specialist at IOtech, has run across distributed measurement applications that were in a relatively small area, but they were too far from the PC to use USB. The customer didn't want to run the strain-gage sensor wires back to a PC, but USB didn't have the distance needed, so Ethernet was the best choice.

The EX-1000A combines 48 temperature or voltage channels with an LXI Ethernet port. Courtesy of VTI Instruments.

New LXI instruments, which use Ethernet, appear on the market regularly. Data-acquisition instruments include those for measuring temperature (see **figure**), strain, and voltage. LXI instruments that support IEEE 1588 let you synchronize measurements across instruments.

Although Ethernet is often the right communications bus for sending measurement data over distances that USB and GPIB can't handle, it sometimes puts engineers face-to-face with the IT staff. "Engineers want to stay away from IT," said Radecky. "IT people don't want engineers plugging things into corporate networks for security reasons."

"Engineers and IT people speak different languages," added Stiernberg. "IT people are also concerned about wireless data acquisition, which uses Ethernet." He also noted that the security protocols used in wireless Ethernet surpass those used in wired Ethernet, so IT staff members may be more concerned with wired measurement applications.

"Engineers need to be network savvy," added Sullivan. "They need to know static IP (Internet protocol) addresses and DHCP (Dynamic Host Configuration Protocol) servers." You may need to set up a subdomain to keep instruments isolated from a corporate network.

Many measurement applications use a network separate from a corporate network. Others may use two network-interface cards on a PC, one for the corporate network and another for the measurement network. "You need a demilitarized zone between measurement networks and corporate networks," added Stiernberg. By isolating your measurement network from a company network, you may keep your IT department at bay, you won't clog the company network with data, and you won't experience delays in getting your data. T&MW

USB data-acquisition modules offer 24-bit resolution

The USB 2416 and USB-2416 AO from Measurement Computing feature 16 differential or 32 single-ended channels with 24-bit resolution. Each can measure voltage or temperature (thermocouples), has eight digital I/O ports, and has two 32-bit counters. The AO version has four analog outputs. www.mccdaq.com.

1-Gsample/s digitizer card uses eight PCIe lanes

Alazar Technologies' ATS9870 features two simultaneously sampled, 1-Gsample/s, 8-bit channels. Using eight PCI Express bus lanes, the card has a sustained bus throughput of 1400 Msamples/s. Acquisition memory is 256 Msamples, 2 Gsamples, or 4 Gsamples. www.alazartech.com.

PCI digitizer cards sample at up to 4 Gsamples/s

The CobraMax series of PCI digitizer cards from GaGe come with one or two channels with sample rates of 3 Gsamples/s or 4 Gsamples/s. Acquisition memory ranges from 256 Msamples to 4 Gsamples. The cards can provide signal processing and data analysis. www.gage-applied.com.

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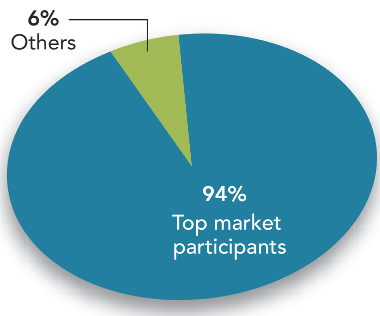
Consolidation: the buzzword in the chip ATE market

The worldwide semiconductor ATE (automatic test equipment) market has witnessed several mergers and acquisitions in recent years. Significant consolidation started as early as 2003 and has not stopped. Some of the key mergers and acquisitions include:

- Credence Systems acquired the assets of SZ Testsysteme in January 2003. The company also acquired NPTest (formerly known as Schlumberger ATE) in May 2004 and merged with LTX in June 2008.
- Teradyne acquired Eagle Test Systems and Nextest Systems in 2008. The company completed the acquisition of Nextest in January 2008 in order to reenter the memory ATE market, and it acquired Eagle Test in November 2008 to enhance its brand recognition and product portfolio.
- Verigy, which was spun off from Agilent Technologies in October 2006, acquired Inovys in January 2008.

As a result of these transactions, the semiconductor ATE market now is dominated by just a handful of companies, including Teradyne, Verigy, Advantest, LTX-Credence, and Yokogawa. The **figure** presents the market share of major participants in the world semiconductor ATE market through 2008.



2008 world market share of the major participants in the semiconductor ATE market.

In addition to mergers and acquisitions, companies have also been focused on developing and introducing new products for the market. Time-to-market is critical in the semiconductor test market, yet finding ways to keep the cost of test low remains the key challenge.

The world semiconductor ATE market registered revenues of $2.43 billion in 2008, declining at the rate of approximately 33% from the previous year. The downfall started in 2007, with most of the companies' revenues declining year on year.

Market growth expects to be driven by DRAM (dynamic random access memory) and flash memory testers, once the economic recovery begins. Sales of mobile phones, PCs, and other consumer electronics also expect to translate into market growth moving forward.

Some of the key criteria for succeeding in the semiconductor test market are to provide comprehensive testing solutions, reduce the overall cost of test, reduce time to market, and increase production yields. A strong focus on R&D for developing and introducing test equipment that can test ever-more complex devices is also a key factor for success in the market today.

So far, 2008 has been the busiest year in terms of consolidation in the semiconductor ATE market. The consolidations have resulted in increased product portfolios and enhancements of existing products. Our research indicated that by 2013, there will be no more than three or four major competitors left in this market space. T&MW

Ultramobile device market heats up

A real dogfight is at hand in the UMD (ultra mobile device) market, not only among various brands but also among different categories within the market, reports In-Stat. Consumers have more choices than ever for untethered Internet connectivity, and with new functionality being added to existing products, the lines of distinction among product categories are blurring. That means the battle for the consumer dollar among MIDs (mobile Internet devices), UMPCs (ultramobile PCs), portable entertainment devices, and smart phones will be fierce.

Details are available in the $1495 report "Mobile Device Update: MIDs & UMDs Face Challenges." www.in-stat.com.

Upsets in semiconductor top 20 ranking

Blaming the economic recession, IC Insights (www.icinsights.com) has reported a major shakeup in the Q1 top 20 semiconductor ranking as compared to the research company's 2008 ranking. Only three of the 20 positions remained the same, with Intel in the catbird seat in the No. 1 top spot, Samsung at No. 2, and Fujitsu retaining the No. 17 rank. See the complete list at www.edn.com/article/CA6658657.html.

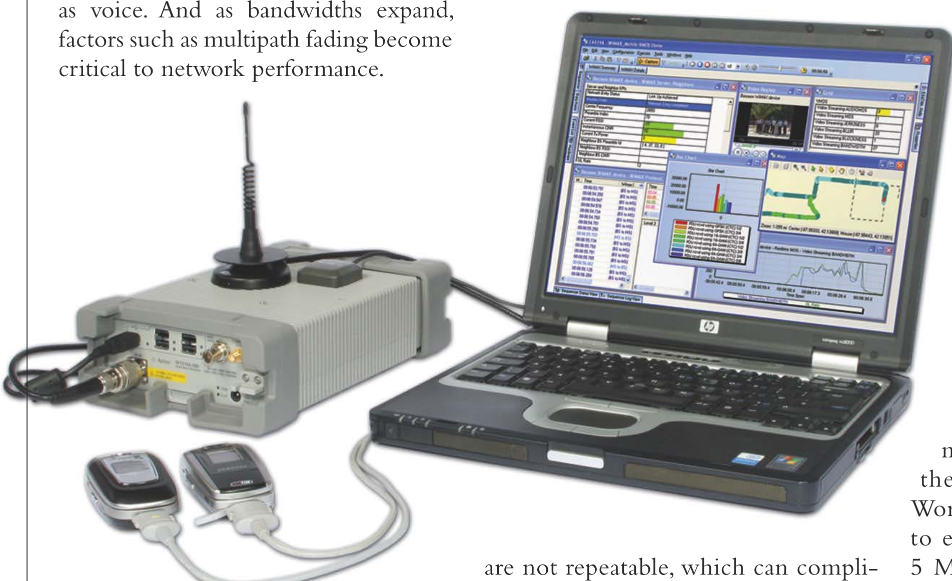
Nearly 800 planes to get in-flight broadband by year end

The number of broadband enabled airplanes will increase from 25 in 2008 to 800 in 2009, reports In-Stat. As a result, broadband-hungry airline passengers will generate over $47 million worldwide in 2009. The in-flight broadband market is still emerging and will grow well beyond $1 billion annually by 2012. "The market is clearly gaining momentum, with deployments escalating in number," said Daryl Schoolar, In-Stat analyst. The $2995 report "Delayed Departure: Will In-Flight Broadband Take Off?" predicts that in-flight broadband equipment revenue will nearly double between 2009 and 2013.

RF TEST

Drive test adapts to VoIP, moves into lab

"Can you hear me now?" So asks the advertising character who personifies the complex drive testing that wireless carriers perform to test the reliability of their networks, monitoring parameters like BER (bit-error rate), FER (frame-error rate), and DCR (dropped-call rate), which in turn affect customer satisfaction (Ref. 1). Drive testing is becoming increasingly important as cellular technology evolves into wideband implementations that carry data as well as voice. And as bandwidths expand, factors such as multipath fading become critical to network performance.



Agilent Technologies has added VoIP capabilities to its drive-test platform; the upgrade addresses carriers' migration to LTE and WiMAX technology.
Courtesy of Agilent Technologies.

To address evolving needs, Agilent Technologies at CTIA Wireless 2009 (Las Vegas, NV, April 1–3) introduced VoIP (voice over Internet Protocol) capabilities for its drive-test system. The system works by generating RTP (real-time transport protocol) streams that mimic VoIP traffic. The software takes time-stamped measurements as the RTP traffic flows between two endpoints in the data network. The measurements include R-Factor MOS (mean opinion score), packet loss, delay, and jitter, and can be automated within the same drive test software that simultaneously performs RF measurements. The VoIP tool works for established mobile data services such as WiMAX, UMTS, and EVDO and will work for LTE when a compliant phone is developed, Agilent reports.

Drive testing is not without its own problems. Although it remains indispensable, real-world drive-test results are not repeatable, which can complicate efforts to troubleshoot dropped-call problems experienced during an actual drive test.

To address that issue, Spirent Communications at CTIA Wireless 2009 announced that it had added virtual-drive-test-capability and fading functionality to its SR5500 wireless channel emulator. Nigel Wright, VP of product marketing, explained that the goal is to let users "capture data in the field that upsets their device and bring it back to the lab," where the emulator enables a single scenario to be played out across multiple test runs within a consistent RF environment.

A key component of Spirent's virtual-drive-test system is the Fading Lab engine, which can simulate channel scenarios for testing MIMO (multiple input, multiple output) and other multiple-antenna systems. In a series of white papers (Refs. 2–4), Doug Reed, solutions architect at Spirent, describes why fading must be considered in modern radio-propagation environments, noting that as bandwidths increase, so does a receiver's ability to resolve multipath signals. He provides details on flat fading, frequency-selective fading, and shadow fading and notes that multiple antennas used in the transmitter, receiver, or both can provide significant performance improvements.

Reed also introduces the SCM (Special Channel Model) developed by the 3GPP (3rd Generation Partnership Project) to emulate real-world multipath conditions in suburban and urban areas, and he describes correlation-based and path-based spatial-channel modeling techniques that can help evaluate multiple-antenna systems' performance. He also covers a proposal in the European WINNER (Wireless World Initiative New Radio) project to extend channel bandwidths from 5 MHz to 100 MHz; the resulting channel model is called SCME (Special Channel Model Extended).

Rick Nelson, Editor in Chief

REFERENCES

1. Mishra, Ajay R., *Fundamentals of Cellular Network Planning and Optimisation: 2G/2.5G/3G...Evolution to 4G,* Wiley, 2004.

2. Reed, Doug, "Correlation-Based Spatial Channel Modeling—White Paper #100," Spirent Communications.

3. Reed, Doug, "Fading Basics: Narrow Band, Wide Band, and Spatial Channels—White Paper #101," Spirent Communications.

4. Reed, Doug, "Path-Based Spatial Channel Modeling: SCM/SCME—White Paper #102," Spirent Communications.

See the online version of this article (www.tmworld.com/2009_06) for links to the Spirent Communications white papers.

SERIAL-BUS TEST

DisplayPort bus demands different tests

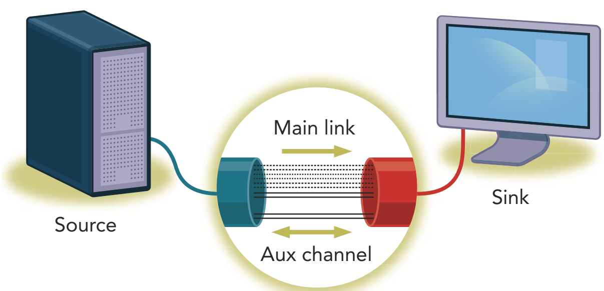
DisplayPort, the serial bus that sends digital video to TVs and monitor screens, needs testing like any other high-speed bus. Timing jitter can affect the BER (bit-error rate) of the bus and produce errors that result in poor video or audio. DisplayPort's architecture, which uses a multilane, unidirectional main link (**figure**) for transferring video and audio, differs from other buses that use bidirectional links. Thus, you can't run loopback tests.

Instead, you must rely on a DisplayPort receiver, called a sink device, to count its own bit errors. A counter in the device counts errors, and you poll the counter through a low-speed bidirectional port called the aux (auxiliary) channel.

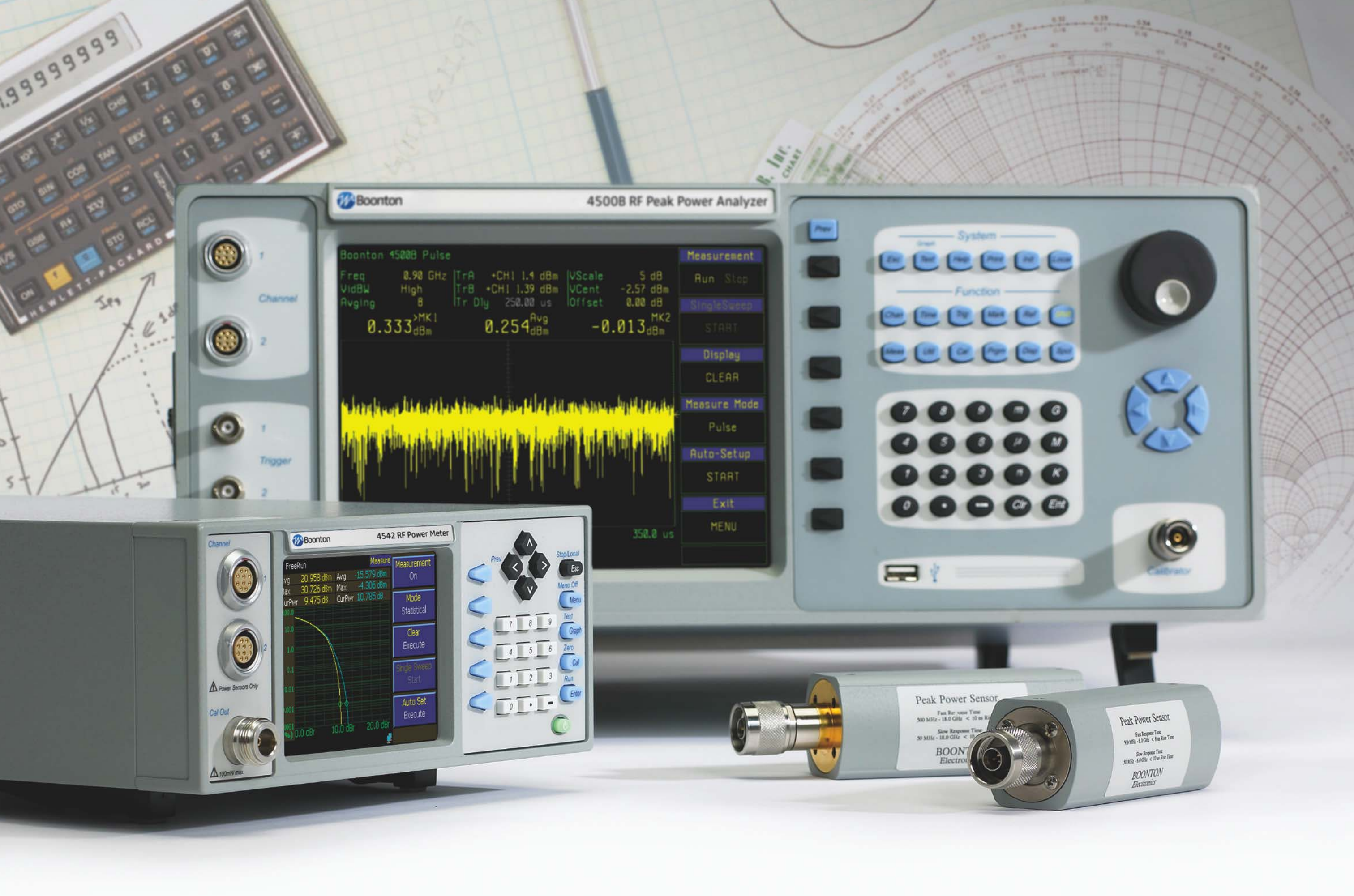
When testing a sink device, you need to inject a PRBS (pseudorandom bit sequence) data stream and add jitter to the stream. Then, you can read the registers of the bit counter. To gain access to the aux channel and to the main link, you need an aux-channel controller board. The board contains connectors to which you can connect a signal from a BER tester or arbitrary waveform generator. Because cables and connectors add jitter and loss to signals, you must compensate for those losses through de-embedding.

To learn more about DisplayPort testing, download "DisplayPort adds testing twists" by Steve Sekel of Synthesys Research from the online version of this article at www.tmworld.com/2009_06.

Martin Rowe
Senior Technical Editor



A DisplayPort link consists of a one, two, or four-lane unidirectional main link and a bidirectional auxiliary channel for control and status monitoring.



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Emulate SPI signals with a digital I/O card

Four I/O lines let you test microcontroller-based products.

By Andy Street, Autoliv Electronics, Lowell, MA

When developing a design-verification tester for millimeter-wave SOC (system-on-chip) devices, my coworkers and I needed to combine switching, electrical measurements, temperature measurement, a parallel digital interface, and a serial digital interface into one instrument. To minimize rack space, we used an Agilent Technologies 34980A multifunction mainframe, which we were already using for DC switching and temperature measurements. By adding an Agilent 34950A 64-bit digital I/O card, we developed a digital interface that emulates both an SPI (serial peripheral interface) bus and a simple parallel bus.

The 34950A groups its I/O lines into two banks of four 8-bit channels. It provides 64 kbytes of memory per bank for pattern generation or signal capture. It also has three I/O lines per bank for handshaking. We found, however, that the card's handshake lines provided insufficient control for implementing SPI transactions. To get the proper control, we emulated the SPI bus using three of the I/O lines.

SPI is a master-slave protocol originally used with Motorola microcontrollers. Today, it's become the control interface in a variety of ICs including PLLs (phase-locked loops) and RF ASICs (Refs. 1, 2). The SPI bus is based on four lines:

- CLK. The clock signal from master to slave. All SPI signals are synchronous with this clock;
- SS. The slave-select line (selects the slave for communication);
- MOSI. The master-out, slave-in data line; and
- MISO. The master-in, slave-out data line (not used in some implementations such as PLL control).

The SPI bus uses one of four possible operating modes that specifies the clock edge used for toggling and sampling and the clock idle level. There is no requirement on voltage levels or data rates, and many SPI implementations can use clock rates greater than 10 MHz.

Figure 1 shows a block and timing diagram of the 34950A bank 1, when configured for synchronous, buffered output where H0 through H2 denote the handshake lines. An illustrative SPI transaction is also shown for reference.

You cannot use the 34950A's handshake lines to emulate all modes of the SPI bus because the bus latches data on the falling edge of the clock, making the bus unsuitable for slaves that use

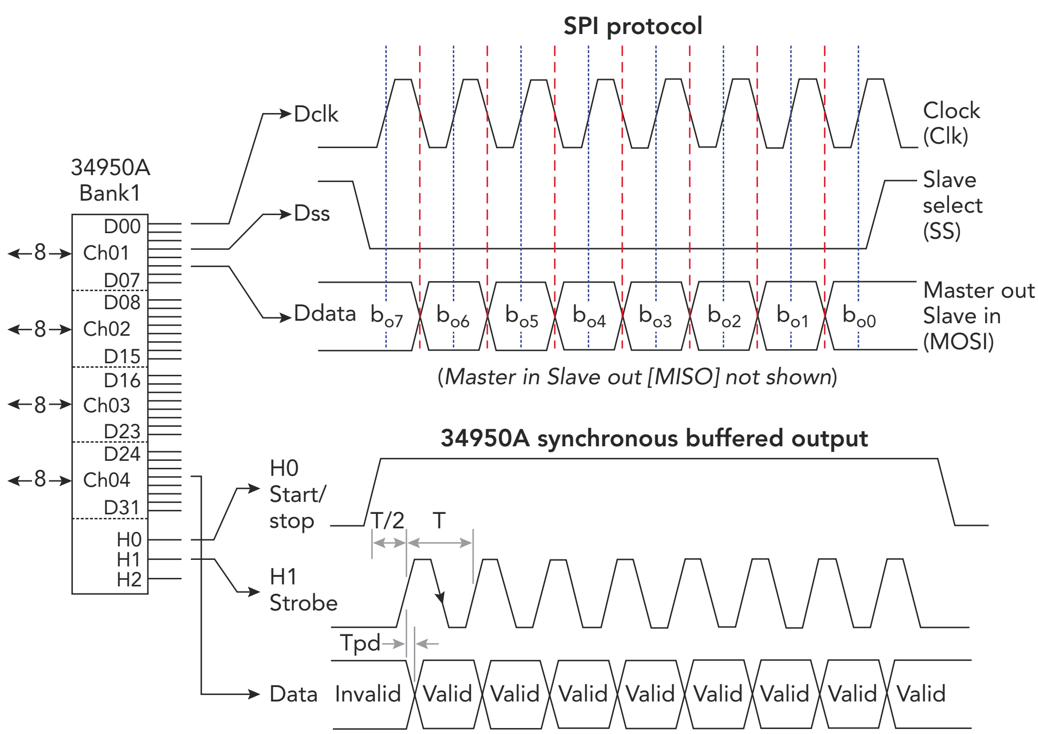

Figure 1 The 34950A synchronous buffered output uses the falling edge, making it unsuited to rising edge SPI implementations.

the rising edge. Inverting the clock polarity is not a solution because the last data bit may be lost. Furthermore, if you write a number of transactions to a slave, you must store each transaction as a separate trace memory in the 34950A.

While each bank can support up to 64k x 8 bits, the number of traces that can be stored is limited to 32. That limits the number of SPI transactions. In addition, the card lacks a sequencer, so you cannot download a number of bit patterns and then play them in sequence. You must load each pattern into the I/O card's memory, and then play each pattern under SCPI control from a host computer. That makes multiple transactions slow.

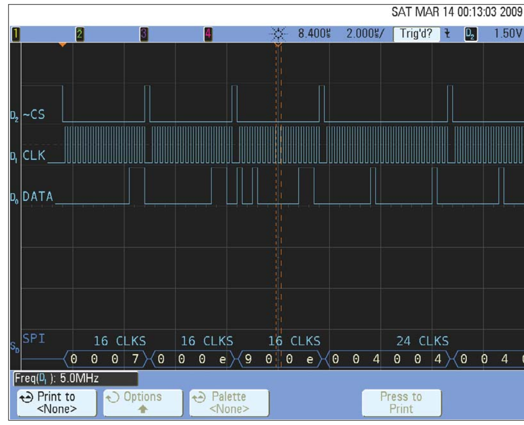

Figure 2 An MSO screen shows the SPI transactions using the digital I/O lines.

Instead of using the handshake lines, we use three of the data lines to emulate the SPI bus. The software driver for the card has to translate the data into an SPI bit stream. The algorithm, expressed in pseudocode below, translates a hexadecimal string, D_H, of characters to an SPI signal. LD, LSS, and LCLK are integers to define which data outputs represent the MOSI, CLK, and SS, respectively.

n_1 = string length of D_H

$n_2 = 8 \bullet n_1$ (# of samples in payload: 4 bits per Hex character, two times oversampling to phase clock)

D_B = binary array representing D_H (array size is $4 \bullet n_1$)

D_{B2} = oversample D_B by a factor of two (array size n_2)

SS = array of 0's of size n_2

CLK = array of alternating 1's and 0's of size n_2

Payload DS = $D_{B2} \times 2^{LD}$ + SS $\times 2^{LSS}$ + CLK $\times 2^{LCLK}$

Set prefix/postfix for SS: PRE = (array of 1's length N_{PRE}) x 2^{LSS} and POST = (array of 1's length N_{PRE}) x 2^{LSS}

Concatenate the arrays PRE, DS, and POST to form SPI signal

Assuming a 24-bit register write with two bits of overhead for the SS prefix and postfix, the 64-kbyte memory could support more than 1000 SPI transactions. The above approach has two additional advantages: The three lines that form the SPI bus are under software control, which provides cabling flexibility, and the implementation can support multiple slaves through the use of additional SS lines.

Figure 2 shows an MSO (mixed-signal oscilloscope) screen that shows the SPI transaction (~CS denotes SS). The SPI clock rate is 5 MHz, which is limited by the internal 10-MHz clock of the 34950A. The different payload sizes correspond to writing data to 16-bit and 24-bit registers within the slave. T&MW

REFERENCES

1. Leens, F., "An Introduction to I²C and SPI Protocols", *IEEE Instrumentation & Measurement,* Vol. 12, No. 1, February 2009. pp. 8–13.
2. "SPI Block Guide V04.01," Freescale Semiconductor, www.freescale.com.

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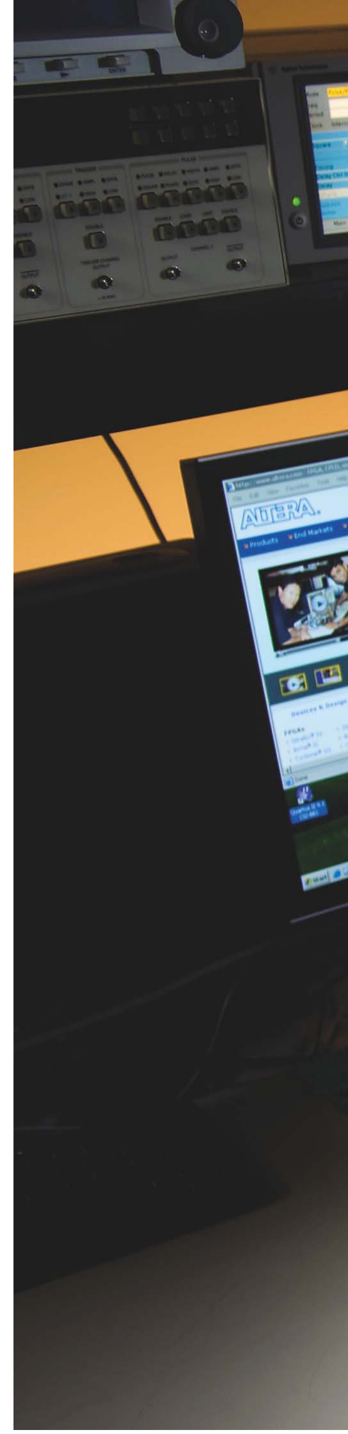


The PHILOSOPHY of JITTER

Signal integrity is key to achieving high-speed serial I/O performance on Altera's 40-nm Stratix IV FPGAs.

BY RICK NELSON, EDITOR IN CHIEF, AND MARTIN ROWE, SENIOR TECHNICAL EDITOR

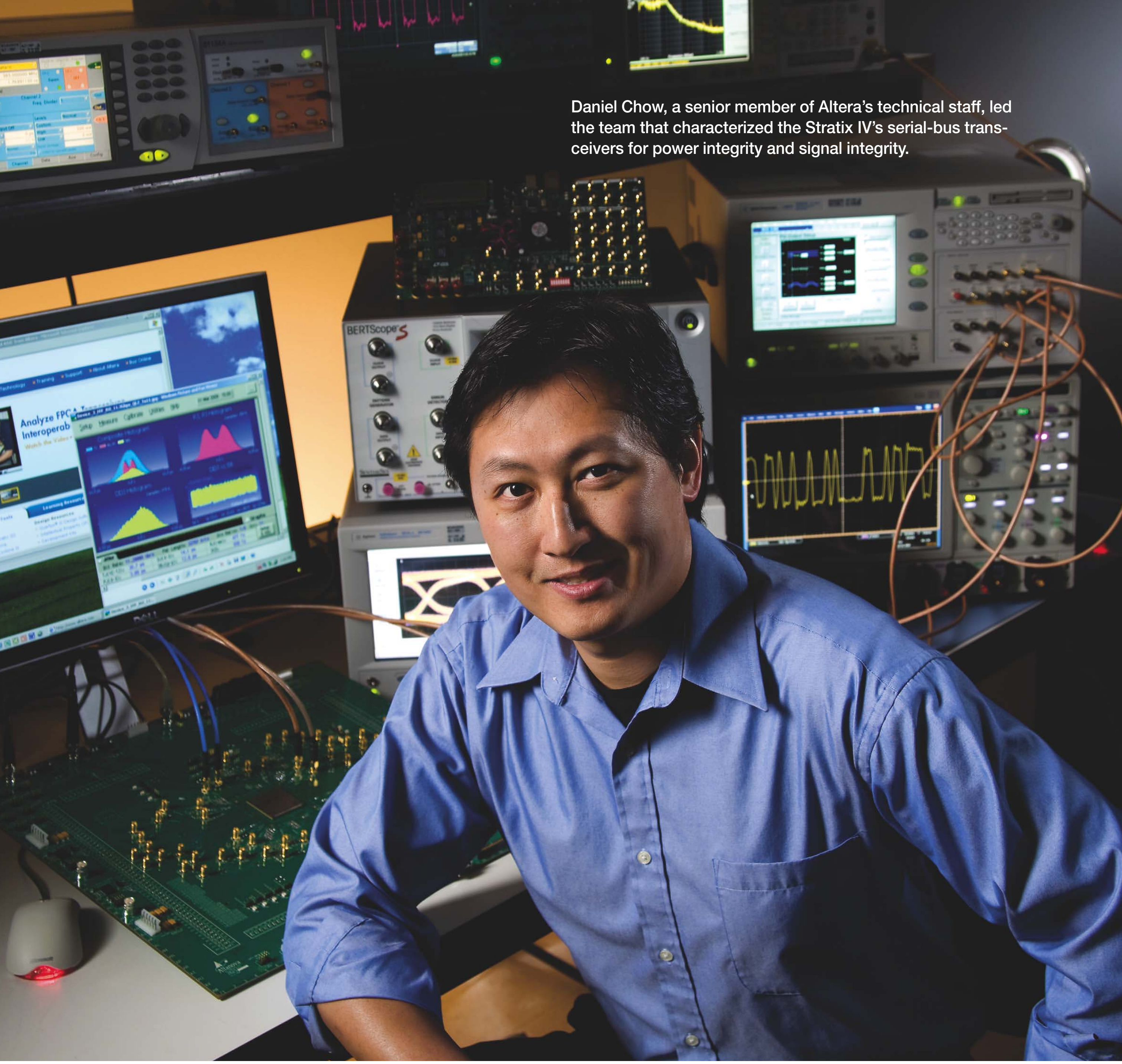
San Jose, CA—When Altera began developing its 40-nm Stratix IV FPGA, the company's engineers faced daunting challenges on many design and test fronts. Their efforts spanned the gamut from working with foundry TSMC in order to perfect the 40-nm process in which the device would be fabricated all the way to developing the software and IP that would allow customers to apply the device.

As Dr. Mike Peng Li, Altera's principal architect and distinguished engineer, put it, the impetus for building the 40-nm parts was to leverage the technological truism expressed in Moore's Law to pack more logic, memory, and interfaces into each chip.

Li explained, "We were able to significantly increase transistor density within Stratix IV as a result of Moore's Law. The higher density reduced the cost per transistor, allowing us to increase the functionality and capability of the device using the same die area. But with the increasing number of transistors per chip, and with FPGAs [field-programmable gate arrays] serving in ultra high-performance applications, such as packet and frame switches, we also needed to increase bandwidth within Stratix IV so data can be rapidly moved in and out of the device."

To do that, Altera had to support the many different flavors of high-speed I/O that its customers might choose to implement, including multiple generations of PCI Express (PCIe 1.1 and PCIe 2.0), Serial ATA/SAS (3 Gbps and 6 Gbps), Fibre Channel (2.125 Gbps, 4.25 Gbps, and 8.5 Gbps), 40/100 Gigabit Ethernet, CEI/OIF (6G and 11G), XFI (10G), and SFI/SFP+. "We had to design the entire hardware protocol stack to enable Stratix IV to support all the different standards," Li said.

EDN executive editor Ron Wilson recently recounted many of the Altera engineers' efforts as they successfully brought to market a device that would earn them *EDN*'s Innovator of the Year award (Ref. 1); in fact, the device itself received an Innovation of the Year award in the "Programmable Logic and Fast-turnaround ASICs" category (www.edn.com/innovation).



Daniel Chow, a senior member of Altera's technical staff, led the team that characterized the Stratix IV's serial-bus transceivers for power integrity and signal integrity.

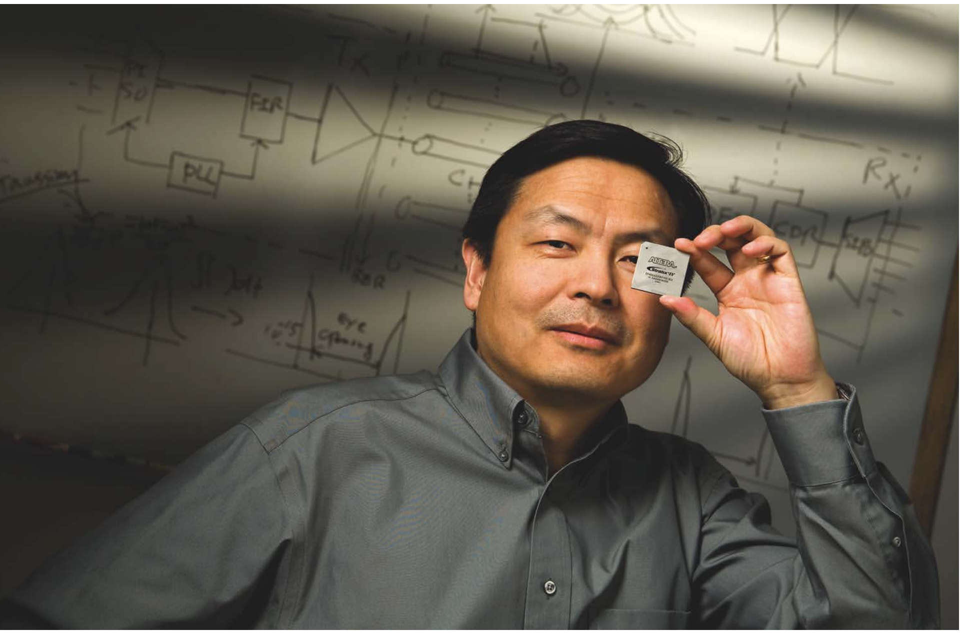
GARY LAUFMAN/GETTY IMAGES

Not surprisingly, some Altera engineers with test responsibilities became the unsung heroes of the development effort, missing out on the honor afforded to the design team. Nevertheless, their efforts were critical as they contended with high-speed serial I/O lines fabricated in new process geometry that pushed speeds to the limits of what commercial test equipment could handle.

Signal integrity

Li noted that high-speed I/O design is becoming more challenging today as speeds increase. "The standards require a bit error rate of 10^{-12} at the physical layer," he said, "and it's getting tougher to maintain that and provide sufficient margin as the UI [unit interval] gets smaller. The implication is that the device-level jitter has to continue shrinking."

Li noted that over the past eight years or so, as transistors have become less expensive, "the communications industry has chosen to put its money in the silicon" to achieve higher speeds, rather than in the cables or PCB (printed-circuit board) materials that make up the rest of the communications channel. He stated, "Silicon today performs functions like pre-emphasis and FEC [forward error correction] on the transmitter side and adaptive equalization on the receiver side to compensate for environmental changes in the channel. Further, some customers want to improve BER [bit-error rate] to 10^{-15} or 10^{-17} so they can forgo functions like FEC,



Dr. Mike Peng Li, Altera's principal architect and distinguished engineer, explained that device-level jitter has to continue shrinking in order to maintain a BER of 10^{-12} at the physical layer while also providing sufficient margin as the UI gets smaller.

thereby potentially reducing power consumption."

According to Li, one way to improve margin is to minimize transmitter jitter. A key source of that jitter, he said, is the VCO (voltage-controlled oscillator) used in the RO (ring-oscillator) PLL (phase-locked loop) that generates

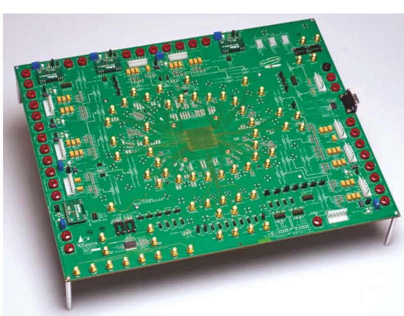


FIGURE 1. A Stratix IV signal-integrity characterization board contains SMA connectors that provide access to an FPGA's high-speed I/O ports. Courtesy of Altera.

clock signals. The RO PLL approach, he said, is useful because it affords customers great flexibility in programming frequencies. But the RO PLL is limited by its phase noise, which can translate into random jitter. To avoid that, Altera offers on its Stratix IV device an LC-based oscillator for its high-performance PLLs, which offers much lower noise and jitter, in addition to RO PLLs.

Power integrity

"In addition to addressing the challenges of signal integrity, we also focused a lot of our attention on power-integrity issues," said Bozidar Krsnik, manager within Altera's characterization team. "Customers are demanding lower power," he said. "Through innovations like our Programmable Power Technology, we became a leader in minimizing FPGA power consumption with Stratix III, and with the Stratix IV we are increasing that leadership. Over the years, we developed the expertise necessary to analyze and characterize power-supply performance and effects as power-supply margins shrink."

Krsnik added, "The power challenges are particularly significant with FPGAs," noting that unlike with ASICs, "customers can do whatever they want in the FPGA fabric. They can create some very unusual worst-case scenarios with respect to power-supply level, clock frequency, and device program pattern." That requires careful analysis on the part of Altera engineers to anticipate what customers might do.

Making the measurements

Many of the test details fell on Daniel Chow, a senior member of Altera's technical staff since 2003. Chow led the team that characterized the Stratix IV's serial-bus transceivers for power integrity and signal integrity, with a heavy emphasis on jitter measurements.

To characterize the high-speed serial transceivers, Altera engineers designed seven types of characterization boards (**Table 1**). With these boards, engineers have access to all of the FPGA's pins, including the power pins that require sources for each of the device's subsystems.

Some functions, especially power integrity, are available in more than one of the boards because power affects all aspects of a device. Plus, if Chow doesn't trust the measurements obtained using one board, he can ask an engineer to repeat the tests with another board.

A characterization board that includes power integrity provides a PDN (power-distribution network) for the FPGA's core, I/O signals, PLLs, differential clock, and high-speed serial transceivers. **Figure 1** shows a characterization board that engineers use for power integrity and transceiver signal integrity. (This is also board 1 in Table 1).

Table 1. Characterization boards for the Stratix IV.

Board number	Uses
1	• Transceiver performance limit • Power integrity
2	• Transceiver (general) • Memory interface • Power integrity
3	• Transceiver (general) • Memory interface • SSN (simultaneous switching noise) • Timing
4	• SSN • LVDS (low-voltage differential signaling)
5	• Automation • High volume
6	• Experimental package design • Power integrity
7	• Protocol validation

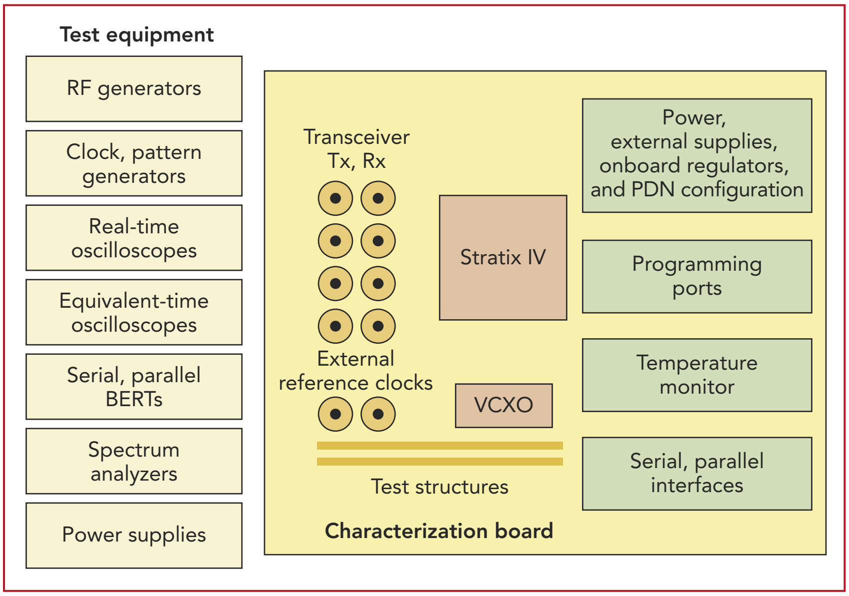


FIGURE 2. This typical test setup shows the instruments used to test I/O port signal integrity and power integrity on the Stratix IV. A characterization board provides engineers with access to the Stratix IV and its transceivers. Courtesy of Altera.

Figure 2 shows a typical setup for testing I/O port signal integrity and power integrity. Test instruments such as signal generators and oscilloscopes connect to the Stratix IV characterization board, providing stimulus and measurements capabilities.

Chow explained why a characterization board needs separate PDN inputs for each FPGA function: "Depending on the customer's applications and requirements, an FPGA might run at optimal performance with all power planes isolated from one another, but it's not always economically feasible to do that. We must recommend to the customer which FPGA sections can share power sources. We want to know how combining power sources can affect signal integrity."

Engineers designing with the Stratix IV might need to isolate power for the device's transceiver buffers and PLL. "You can't always share a power supply if there's too much activity on it," Chow noted. "Power-supply configurations strongly depend on customer applications and requirements; it's our job to find the tradeoffs for different power-supply configurations."

Chow and others characterized the transceivers using both separate and common power supplies. From their tests, they saw how combining power supplies affects signal integrity. For example, transmitters or receivers that pull down the clock's power too much can add too much jitter to transmitted signals.

The Altera engineers also characterized the Stratix IV devices over wider DC voltage ranges than the company recommends to customers. They tested the transceivers at voltages from 0.9 V to 1.4 V before publishing the recommended range of 1.15 V to 1.25 V, and they also tested the Stratix IV across a wide temperature range and across semiconductor process corners.

Signal integrity is critical in serial links. Altera's signal-integrity characterization board is made from the finest PCB materials and SMA connectors that the engineers could find. Why? Because they must minimize voltage losses and jitter that traces and connectors can add so that the results are more representative of the device's intrinsic behavior. Note the varying distances of the SMAs to the FPGA in Figure 1. Engineers use the SMA connectors with the shortest traces to test the transceivers under electrically quiet conditions, which minimizes signal degradation.

Testing in a quiet environment lets Altera engineers know how well a device can perform, but it doesn't provide data on real-world performance. How a customer uses the core, logic, and I/O sections of the device affects transceiver performance, especially at high data rates. Thus, Altera engineers must characterize the device under numerous operating configurations.

The company's characterization engineers don't start by simply exercising

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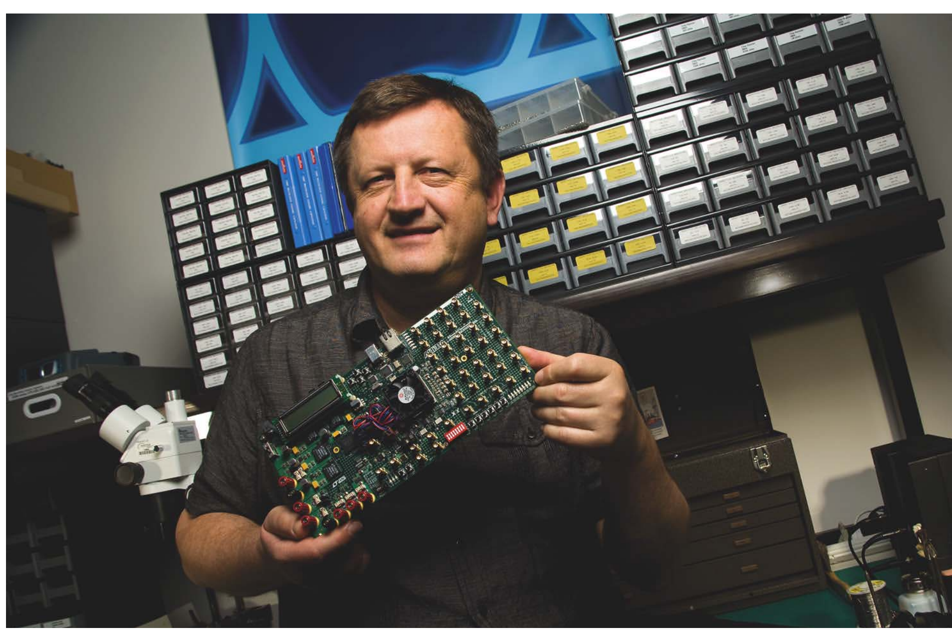

"In addition to addressing the challenges of signal integrity, we also focused a lot of our attention on power-integrity issues," said Bozidar Krsnik, manager within Altera's characterization team. "Customers are demanding lower power."

every gate and I/O pin. That's unrealistic because no customer will use every transistor in an FPGA. "Every one of our customers uses our FPGAs differently," noted Chow. "So, we get sample designs from customers and learn how they use our parts." Once they know how a customer uses the part, Altera engineers emulate the customer's application, but not right away.

Altera engineers gradually move from testing in a quiet environment to a realistic one. They may start with just one transceiver, then gradually turn on adjacent transceivers while looking for crosstalk and jitter with unpowered FPGA core logic circuits and I/O pins.

After running the transceivers, the engineers begin exercising the FPGA's I/O pins while looking to see how that affects the PDN and signal integrity. They then turn on the core and logic sections and review the transceiver signals. Each time the engineers turn on a portion of the device, they check the power integrity, looking for noise and voltage dips, which has a profound impact on PLLs and signal jitter.

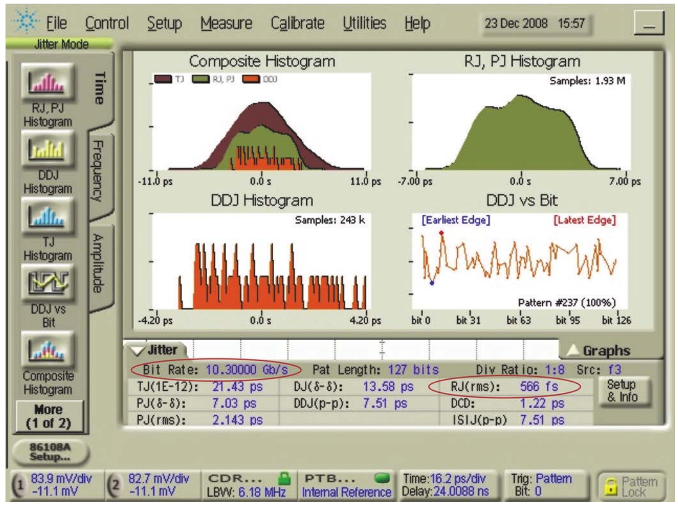

FIGURE 3. At 10.3 Gbps, a Stratix IV serial I/O port achieves RJ (random jitter) of 566 fs. Courtesy of Altera.

The study and characterization of jitter is central to Chow's work. "Ten years ago, we were blind," he said. "We didn't understand jitter the way we do today. We didn't know about TJ [total jitter], RJ [random jitter], DJ [deterministic jitter], PJ [periodic jitter] or ISI [intersymbol interference]. As Fibre Channel and XAUI came online, we began to understand jitter. Mike Peng Li was one of the first to realize that TJ only mattered when you specified BER."

To measure jitter, Chow and other Altera engineers use an array of instru-

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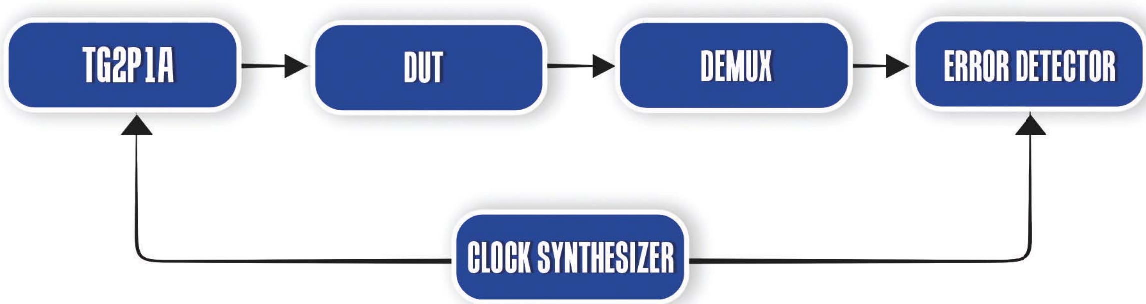

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ments such as real-time and sampling oscilloscopes from Agilent Technologies, LeCroy, and Tektronix. In the lab, the engineers also use Agilent spectrum analyzers and BERTs (BER testers) from Agilent and Synthesys Research.

Chow uses so many instruments because each looks at jitter in a different way. He cited the legend of the blind men touching an elephant to illustrate the challenges in measuring jitter. "Imagine that you're blindfolded and you touch part of an elephant from which you try to figure out what you're touching. If you touch the trunk, you might think it's a snake. If you touch a leg, you might think it's a tree. If you touch an ear, you might think it's a fan. Each type of instrument lets you see part of the jitter."

He noted that oscilloscopes measure jitter in the time domain, spectrum analyzers use the frequency domain, and BERTs use the digital domain. Chow uses spectrum analyzers to look at PJ because this jitter component contains frequencies that the instrument can easily display. He also likes using a spectrum analyzer for measuring RJ because it measures phase noise and converts the results into RJ. Spectrum analyzers also have a low noise floor, as low as −160 dBm, which Chow likes for measuring RJ over a specified bandwidth.

Daniel Chow uses a variety of spectrum analyzers, oscilloscopes, and BERTs because "each instrument sees a different part of the metaphorical elephant."

"RJ is getting quite small," he said, noting that standards such as those for SFP and SFP+ transceiver modules specify approximately 800 fs of noise. "For Stratix IV devices, customers can typically expect RJ values between 600 fs and 700 fs. In the lab, we've been able to measure RJ as low as 400 fs. Few instruments can measure RJ below 1 ps. Real-time oscilloscopes are getting there." **Figure 3** shows RJ and PJ on a sampling oscilloscope, where RJ = 566 fs.

With a real-time or sampling oscilloscope, Chow measures DJ, RJ, PJ, and ISI. He measures TJ with a BERT at 10^{-12} BER. If all jitter measurements are properly done, the jitter components should approximately equal TJ.

Chow admitted that sometimes, the jitter components don't add up to the TJ. "These inconsistencies are sometimes due to the instrumentation, which is why we must understand how each instrument derives its jitter results, including hardware limitations, software implementation, algorithms, and jitter theory,"

said Chow. "We do that because each instrument sees a different part of the metaphorical elephant." When the jitter components don't add up, Chow and his team will review their measurement procedures, and they may have to try again using a different oscilloscope or clock-recovery system.

Chow may change oscilloscopes and retake measurements because as data rates have increased to 8 Gbps, 10 Gbps, and 11.3 Gbps, he gets different results for each rate. He noted that 10 years ago he had the same problem, but over time, oscilloscope makers have improved their instruments to the point where differences in jitter numbers can come within 10% of each other at data rates up to about 5 Gbps (Ref. 2). At higher data rates, Chow has seen increasing difference among manufacturers

Chow cited the reasons for the divergence: smaller UIs, which produce smaller jitter margins, and faster rise and fall times. "Instrument makers are constantly telling us that we need more bandwidth in our measurements," said Chow. "Some have suggested that we need a 50-GHz module for a sampling oscilloscope, based on the rule of thumb that we need five times the data rate in bandwidth." But Chow questions if he can truly see a 10-Gbps signal on his oscilloscope anyway. That's because PCB traces and connectors will slow a signal's transition times. "Besides," he noted, "equipment is very expensive. Our job is to figure out which metrics we have to push and what equipment we really need."

Even if Altera had the latest test equipment, its customers often don't. Customers will try to verify the Stratix IV's specifications, and they may lack the right equipment. As a result, Chow and his engineers have to train field applications engineers in how to properly take the measurements. He's received reports from the field where customers measured jitter with oscilloscopes that lack sufficiently low noise floors to measure Stratix IV's low jitter performance. Customers will claim that they don't get jitter measurements that are consistent with Altera's; the field engineer must explain that the problem is in the measurement equipment or setup, not necessarily in the device.

Engineers at Altera have indeed figured out how to test and characterize the Stratix IV FPGA. Now, it's up to their customers to design and test communications products with standard and proprietary protocols that take advantage of the device's serial I/O capabilities. T&MW

REFERENCES

1. Wilson, Ron, "Bringing giant FPGAs to a new node," *EDN Innovators 2009*, March 2009. p. 5. www.edn.com/article/CA6643372.html.

2. Chow, Daniel, and Ransom Stephens, "Methodology for Jitter Measurement Correlation and Consistency," Proceedings from DesignCon 2005. www.designcon.com/media/2005/East/1-TA4--Daniel_Chow.pdf.

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Small-delay-defect TESTING

SDD automatic test-pattern generation breaks the nanometer quality barrier.

Semiconductor companies have come to rely on delay testing to attain high defect coverage of manufactured digital ICs. Delay testing uses TD (transition delay) patterns created by ATPG (automatic test-pattern generation) tools to target subtle manufacturing defects in fabricated designs. Although TD ATPG improves defect coverage beyond the levels that stuck-at patterns alone can achieve, the methodology is limited in its ability to reach the test quality levels required for nanometer designs. As a result, STMicroelectronics is deploying a new delay test methodology called SDD (small delay defect) ATPG as a means to achieve even higher defect coverage than standard TD ATPG.

Why SDDs?

"Delay defect" refers to any type of physical defect, or an interaction of defects, that adds enough signal-propagation delay in a device to produce an invalid response when the device operates at the targeted frequency. Experimental data going back two decades (Refs. 1 and 2) have shown that the distribution of delay-related failures is skewed toward the smaller delays. That is, the majority of devices that fail due to delay defects fail because of "small delay defects" that contribute to delays much smaller than the clock cycle times associated with the process technology node. Targeting these SDDs during test improves defect coverage and lowers the test escape rate, measured as DPPM (defective parts per million).

On-chip process variations are more pronounced in today's manufacturing processes because of the increased presence of systematic defects—stemming from complex interactions between lay-

BY ROBERTO MATTIUZZO AND DAVIDE APPELLO, STMICROELECTRONICS, AND CHRIS ALLSUP, SYNOPSYS

out, mask manufacturing, and wafer processing—compared with previous process technologies (Ref. 3). These process variations tend to further skew the delay-failure distribution toward smaller delays, adding enough incremental signal delay to adversely impact circuit timing in a higher percentage of devices. In essence, for a given die size, the product yield of a 45-nm design can decrease sufficiently over that of a 90-nm design that manufacturers must boost the coverage of SDDs just to maintain about the same DPPM levels observed for the 90-nm process.

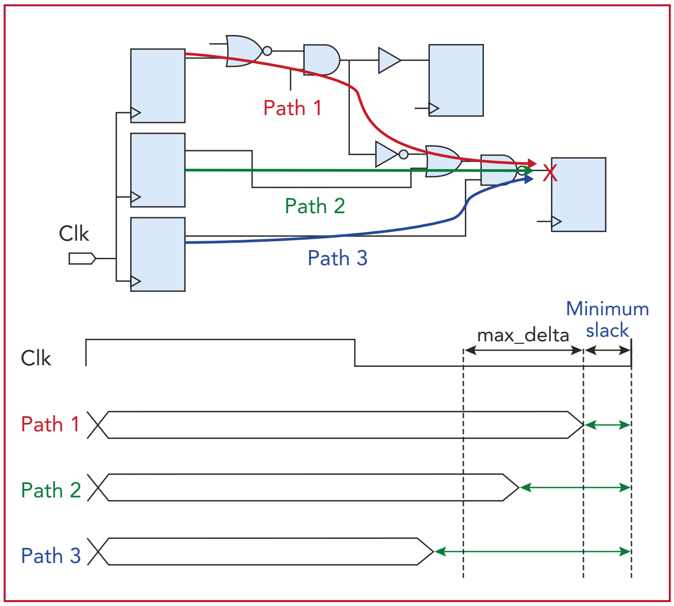


FIGURE 1. Coverage of small delay defects depends on the fault's path of detection and the amount of slack in that path (indicated by the green arrows). Here, path 1 exhibits the minimum slack.

Limitation of TD testing

So, why doesn't standard TD testing cover SDDs? In fact, it does cover some of them, but not enough to achieve the quality levels required at STMicroelectronics, which is pursuing a strategic quality objective of zero DPPM.

The traditional goal of ATPG tools has been to minimize run time and pattern count, not cover SDDs. TD ATPG targets delay defects by generating one pattern to launch a transition through a delay fault site—which may activate either a slow-to-rise or a slow-to-fall defect—and by generating a second pattern to capture the response. During testing, if the signal doesn't propagate to an end point (a primary output or scan flop) in the at-speed cycle time, then incorrect data is captured. In this scenario, the pattern sequence detects a delay defect through the activated path.

To minimize run time and pattern count, TD ATPG uses a "low-hanging fruit" approach to targeting transition delay faults: It targets them along the easiest sensitization and detection paths it can find, which often are the shortest paths. To understand how this affects SDD coverage, consider the circuit in **Figure 1,** which shows three possible detection paths for a single delay fault. TD ATPG typically generates a pattern sequence that targets the fault along the path that has the largest timing slack, path 3. Notice this pattern sequence doesn't cover smaller delay defects associated with path 1 and path 2 that would have been covered by targeting the path with smallest slack, path 1.

TD ATPG does manage, however, to detect some SDDs, either directly as targeted faults or indirectly as bonus faults when targeting other faults. Even so, TD ATPG rarely detects delay faults along the longest paths needed to detect defects of the smallest "size" (that is, delay).

In summary, TD ATPG is effective for detecting delay defects of nominal and large size, but because it doesn't explicitly target delay faults along the minimum-slack paths, it's not effective in detecting delay defects of relatively small size.

SDD ATPG

SDD ATPG, in its purest form, is similar to path-delay testing. It targets each undetected fault along the path with minimum timing slack. In Figure 1, path 1 has the minimum slack, so the pattern generator will target the fault through path 1. If the fault is detected, it is categorized as DS (detected by simulation). The fault simulator also classifies bonus faults as DS if they're detected along their minimum-slack paths.

If any fault—a targeted fault or a bonus fault—is detected along a path shorter than its minimum-slack path, it is designated as TP (transition partially detected). A TP fault will continue to be fault-simulated each time ATPG generates a new pattern in hopes that a pattern will eventually be generated that detects, as a bonus fault, this same fault through its minimum-slack path. The main drawback with this method is that, in the process of targeting every undetected fault along its minimum-slack path, SDD ATPG wastes time and patterns working on faults that don't contribute to detecting SDDs.

To illustrate, **Figure 2** represents the histogram of all TD faults in a hypothetical design, with the faults normally distributed according to their minimum slacks. For each discrete value of slack on the horizontal axis,

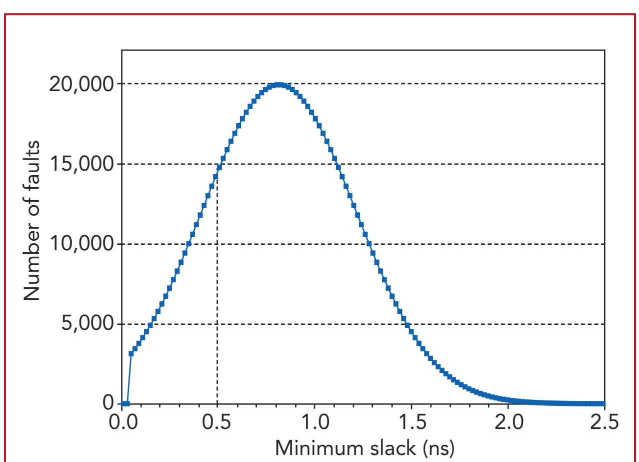
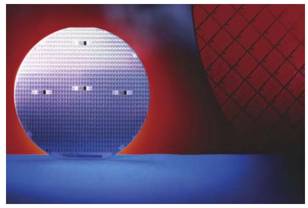


FIGURE 2. This sample histogram of transition delay faults in a design shows faults distributed according to minimum slacks.

a certain number of faults in the design have this value as their minimum slack. As the vertical dotted line indicates, there are nearly 15,000 faults in the design with minimum slack of 0.5 ns. Some 200,000 faults, or 20% of the total, have minimum slack less than or equal to 0.5 ns. Targeting faults with minimum slack in this lower range is an effective way to test for SDDs. On the other hand, targeting faults with much higher minimum slacks doesn't detect SDDs; the slacks of these faults are large enough that standard TD ATPG covers them very efficiently.

A hybrid approach to pattern generation uses SDD ATPG to target faults having relatively small minimum slack along their minimum-slack paths and uses TD ATPG to target the remaining faults along their easiest-to-detect paths. Synopsys' TetraMAX ATPG product (Ref. 4) uses a parameter called max_tmgn (the maximum timing margin) to assign the cutoff slack level for targeting faults at their minimum slacks. Faults along paths with minimum slack less than or equal to max_tmgn will be targeted by SDD ATPG algorithms, while other faults will be targeted by TD ATPG algorithms.



One approach to reducing pattern count is to "cut ATPG some slack."

When the minimum slack of a detected fault exceeds the maximum timing margin, the fault will be classified as TP even if the fault is detected along its minimum-slack path. Narrowing the scope of SDD ATPG to focus on what it does best—testing for the smallest delay defects—reduces both pattern count and run time significantly.

Reducing pattern count

In some situations, it may be beneficial to further reduce the pattern count of SDD ATPG. One approach is to "cut ATPG some slack" by letting it generate a pattern that can still detect small (though not always the smallest) delay defects related to a fault. TetraMAX ATPG uses a parameter, max_delta, to control this behavior. If the slack of the detection path for a fault exceeds the fault's minimum slack by not more than the value of the max_delta parameter, then the fault simulator will classify the fault as DS.

Referring again to Figure 1, if ATPG cannot detect the targeted fault through its minimum-slack path, path 1, it will attempt to target the same fault through a path with larger slack. As indicated in the timing diagram, the slack of path 2 is less than the sum of the fault's minimum slack and the value of max_delta, so detecting the fault along path 2 will cause the fault simulator to classify the fault as DS. The slack of path 3, however, exceeds the minimum slack of the fault plus the value of max_delta, so detecting the fault along this shorter path will cause the fault simulator to classify the fault as TP.

Increasing max_delta above its default value of zero reduces pattern count because more faults per pattern pass the criterion for DS classifications, and fewer faults need to be targeted by ATPG in each subsequent pattern. Moreover, with each succeeding pattern generated, there are fewer and fewer TP faults for the fault simulator to keep track of, so the simulation run time decreases. A non-zero value of max_delta, however, reduces delay effectiveness.

Delay effectiveness

Delay effectiveness is a coverage metric used to quantify how successfully patterns detect faults through their longest paths. Only faults that are detected along paths having slacks less than or equal to max_tmgn contribute to delay effectiveness. These can include both DS and TP faults. TP faults can contribute to delay effectiveness because a fault could be detected along a path with slack less than max_tmgn, even though the

Minimum slack

Delta	0.04	0.06	0.08	0.10	0.12	0.14	0.16	0.18	0.20	0.22	0.24	0.26	0.28	0.30	0.32	0.34	0.36	0.38	0.40	0.42	0.44	0.46	0.48	0.50	0.52	0.54	0.56	0.58	0.60
0.00	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.02	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.04	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.06	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.08	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.10	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.12	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.14	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.16	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.18	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.20	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.22	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.24	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.26	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.28	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.30	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.32	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.34	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.36	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.38	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.40	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.42	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.44	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.46	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.48	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.50	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.52	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.54	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.56	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.58	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.60	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP

FIGURE 3. A detected fault contributes to delay effectiveness depending on the ATPG parameters max_tmgn and max_delta, and the slack of the detection path. In this example, max_tmgn = 0.5 ns and max_delta = 0.3 ns. The fault is classified as a DS or TP fault depending on the fault's minimum slack, the additional slack needed to detect the fault (delta), and the ATPG parameters. The red-shaded combinations contribute to delay effectiveness.

slack exceeds the minimum slack of the fault plus the value of max_delta.

Figure 3 illustrates how a single detected fault can contribute to delay effectiveness depending on the slack of its detection path and the parameters max_tmgn and max_delta, which are assumed to be 0.5 ns and 0.3 ns, respectively, in this example. The slack of the detection path is simply the sum of the minimum slack of the fault (horizontal axis) and the additional slack needed to detect the fault, referred to as "delta" (vertical axis).

The entry for each combination of minimum slack and delta indicates whether the detected fault is of type DS or TP, with red-shaded entries representing those combinations that result in the fault contributing to delay effectiveness. The sidebar "Test effectiveness" in the online version of this article (www.tmworld.com/2009_06) describes how to calculate test coverage and delay effectiveness for SDD testing and explains how the ATPG parameters max_tmgn and max_delta affect these metrics.

Timing is everything

SDD testing is feasible only if the ATPG tool can make efficient decisions—often thousands per pattern—based on accurate timing information about the design. Yet, the need to dynamically perform timing calculations inside the ATPG tool (based on Standard Delay Format data, for example) compromises run-time performance and can produce results that don't correlate well with sign-off timing analysis.

TetraMAX ATPG avoids these issues by accessing data generated by Synopsys' PrimeTime static timing-analysis tool. PrimeTime models all the key process, physical, noise, and clock network effects required for accurate timing analysis of nanometer designs, so it helps TetraMAX ATPG target SDDs.

Two basic kinds of timing information are required for SDD ATPG: slack data and timing exception data. **Figure 4** depicts the four-step flow for generating this information:

1. Standard Test Interface Language (STIL) procedure file (SPF) describes the test-mode protocols for launch and capture.

2. The TetraMAX ATPG DRC (design rule checker) interprets the launch and capture timing requirements and produces an SDC file that defines the launch- and capture-mode timing constraints.

3. (a) PrimeTime interprets the launch- and capture-mode timing constraints and produces an SDC file that defines the test-mode timing exceptions, and **(b)** PrimeTime generates a report containing the test-mode timing slacks for each fault site.

4. TetraMAX ATPG reads in the slack and timing exception information produced by PrimeTime to generate SDD patterns.

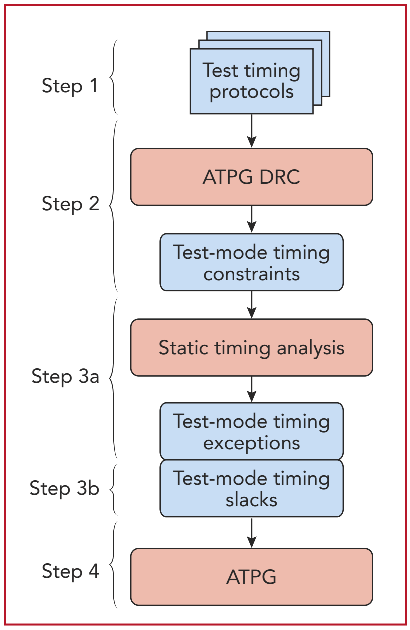


FIGURE 4. The flow for generating slack data and timing exception data for SDD ATPG involves a four-step process.

The correct processing of timing exceptions is essential to both SDD ATPG and standard TD ATPG; the combined flow for SDD testing differs only in the requirement to import slack data from PrimeTime to TetraMAX ATPG (step 3b). The flow ensures that the design's timing constraints reflect the test-mode launch and capture timing, which differs fundamentally from mission-mode timing.

Silicon testing results

The Synopsys flow for SDD pattern generation is now supported in the sign-off methodology at STMicroelectronics, where SDD testing is considered key to reducing DPPM levels across the company's product lines. The company has found that SDD testing offers improved product quality over standard TD testing (or any other type of test in use today), as evidenced by failure statistics collected for an automotive IC that STMicroelectronics designed and manufactured. The design, consisting of approximately 1 million equivalent gates, was manufactured in a 90-nm CMOS process.

Figure 5 displays a Venn diagram of data collected from testing hundreds of thousands of parts using four fundamental types of tests: stuck-at, static bridging, dynamic bridging, and delay tests. The delay tests were composed of standard TD patterns and SDD patterns. The data indicate that about 94.5% of all failing parts were covered by the delay tests, and that 20% of failing parts were covered *only* by the delay tests.

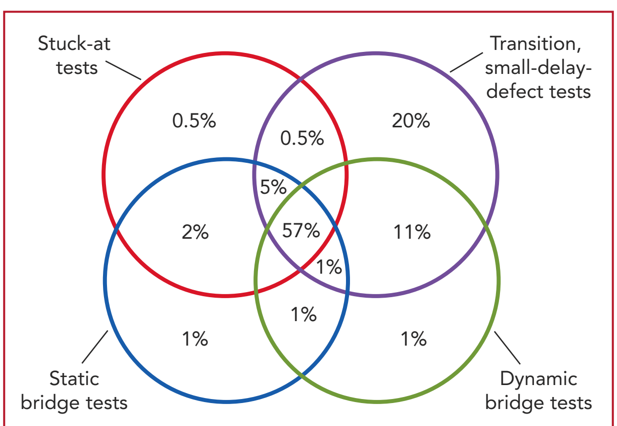


FIGURE 5. This Venn diagram shows the percentage of failing parts covered by each type of test.

Upon examining the data for the 20% of defective parts covered only by the delay tests, we observed that 63% of these parts were covered *only* by the

SDD patterns. The remaining 37% covered by TD patterns were also covered by SDD patterns. Test engineers at STMicroelectronics have observed results similar to these for other designs; SDD tests consistently screen more failures than any other type of production test in use at STMicroelectronics, reducing DPPM levels relative to rates achievable using standard TD tests.

ON THE **WEB**

See the sidebar "Test effectiveness" in the online version of this article to learn how to calculate test coverage and delay effectiveness for SDD testing. The sidebar also explains how the ATPG parameters max_tmgn and max_delta affect these metrics. **www.tmworld.com/2009_06**

Small delay predictions

Recent advances in design-automation technologies have made it possible for semiconductor companies to efficiently target SDDs during manufacturing test. This development has ensured that, in spite of Moore's Law, very high defect coverage will be achievable on a consistent basis in the years ahead: We expect designers will increasingly adopt SDD testing as the primary means to maintain low DPPM levels as they take advantage of ever-smaller geometries to squeeze more functionality on a chip. T&MW

REFERENCES

1. Nigh, P., and A. Gattiker, "Test Method Evaluation Experiments & Data," *Proceedings of the International Test Conference*, *2000,* www.ieee.org. pp. 454–463.

2. Park, E.S., M.R. Mercer, and T.W. Williams, "Statistical Delay Fault Coverage and Defect Level for Delay Faults," *Proceedings of the International Test Conference, 1988*, www.ieee.org. pp. 492–499.

3. Braun, A.E., "Pattern-Related Defects Become Subtler, Deadlier," *Semiconductor International*, June 1, 2005. www.semiconductor.net.

4. TetraMAX ATPG User Guide, Version B-2008.09, Synopsys, www.synopsys.com.

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Field meter adds digital memory

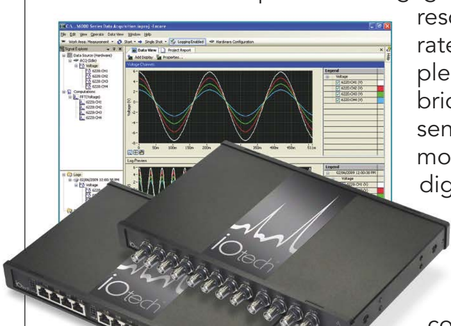
The Smart Fieldmeter Digital from EMC Test Design measures electric fields from 200 kHz to 18 GHz, depending on which attachable probe you use. The Digital version adds support for an SD memory card, which lets you store data for downloading into a PC. A 1-Gbyte card can store up to 100,000 samples. A memory card, provided with each probe, also keeps the probe's correction factors so you can use any probe with any Smart Fieldmeter Digital instrument. The meter also features an optional RS-232 port with a wired or fiber-optic connection.

The instrument displays and stores measurements in volts per meter or watts per meter. It can automatically take measurements at intervals from 30 ms to 30 min. Each unit comes with a 10-V/m, 1.4-MHz field gauge that lets you check measurements against a reference standard in the field. The meter can run for up to 20 hours on a battery charge using two AA batteries.

Price: $3700. *EMC Test Design, www.emctd.com.*

Connect voltage and strain through Ethernet

IOtech's 6000 series of networked data-acquisition systems consists of models for measuring voltage or for use with strain gages. The Model 6220 accepts 12 simultaneously sampled voltage inputs (±10 V) with 16-bit resolution. Sample rates reach 100 ksamples/s. The Model 6224 accepts 12 strain-gage inputs with 24-bit resolution, sampling at rates up to 50 ksamples/s. It supports half-bridge and full-bridge sensor circuits. Both models have eight digital I/O channels that you can use to trigger alarms or controls.



Both models also come with IOtech's Encore software, which lets you control one or more instruments over a network. You can configure each channel to acquire data and store data on a Windows-based PC. You can plot data and store measurements in formats that are compatible with ASCII text files, Microsoft Excel, and National Instruments' DIAdem. You also can assign signal names, engineering units, and time-stamp data to each channel. Signal-analysis functions include peak, RMS, FFT, and power spectrum.

Prices: Model 6220—$2999; Model 6224—$4799. *IOtech, www.iotech.com.*

Test socket gets adjustable pressure pad

Aries Electronics now offers its 27-mm CSP/MicroBGA (chip-scale package/micro-ball-grid array) test and burn-in sockets with an optional adjustable pressure pad. With only a 0.010-in. (0.254-mm) displacement per revolution of the screw, this mechanism makes the sockets suitable for testing devices with large height tolerances as well as for testing small, fragile devices (such as thin or ceramic chips) without causing damage.

Users can back off the adjusting screw and close the socket's lid securely with one finger and very little force, and then modify the pressure pad force with the adjusting screw to ensure good contact. The screw can also be adjusted based on device height from chip to chip, eliminating socket rework downtime to design a new pressure pad.

Each adjustable pressure pad comes with a user-adjustable washer stack in 0.001-in. (0.0265-mm) and 0.010-in. (0.254-mm) increments that serves as a hard stop to eliminate device over-compression. If constant large device height changes are expected during testing, the washer stack can be removed without affecting the socket's performance.

The Aries CSP/MicroBGA test and burn-in socket family accommodates a variety of CSP, MicroBGA, DSP, LGA, SRAM, DRAM, and flash devices from 6.5 mm^2 to 55 mm^2 by using machined or custom-molded pressure pads and interposers. Signal path is only 0.077 in. (1.96 mm). Contact forces are 15 g per contact on a 0.30-mm to 0.35-mm pitch, 16 g per contact on a 0.40-mm to 0.45-mm pitch, and 25 g per contact on pitches of 0.50 mm or larger. Operating temperature is –55°C to +150°C, and estimated contact life is a minimum of 500,000 cycles.

Price: pressure-pad option—$60 per pad for socket quantities of 50 or more. *Aries Electronics, www.arieselec.com.*

ScanWorks supports Intel Xeon processor 5500 series

Asset InterTech's ScanWorks platform for embedded instrumentation now supports both signal-integrity design validation and circuit-board test for the new Intel Xeon processor 5500 series, code-named Nehalem, as well as the 5520 chipset. The Xeon 5500 series processors will be deployed in systems using Intel's QPI (QuickPath Interconnect) platform architecture.

To validate Intel Xeon processor 5500 series-based designs, the ScanWorks platform employs Intel's IBIST (Interconnect Built-In Self-Test) embedded instrumentation technology, which is being placed in Intel's next-generation processors and chipsets. ScanWorks employs the embedded IBIST instrumentation to perform margining and BERT (bit-error-rate test) on high-speed buses like QPI and PCIe. The same ScanWorks platform with its processor-controlled test capabilities can also test Nehalem-based circuit boards.

ScanWorks is able to take control of an Intel Xeon processor 5500 series CPU and assert structural and functional tests and diagnostics on other devices and buses on the circuit board, including the 5520 chipset. ScanWorks' validation and test capabilities improve the quality of the system and accelerate a new product's time-to-market.

Base price: $13,350. *Asset InterTech, www.asset-intertech.com.*

Record/playback system handles 500 Mbytes/s

You can use the RTS 2701 recording and playback system from Pentek as a test instrument, as a remote data-acquisition system, or as a record/playback subsystem for deployed applications. The dual-channel system provides recording and playback rates of up to 500 Mbytes/s in a 19-in. rack-mount server chassis.

The RTS 2701 can digitize analog signals from a communications system or radar system and deliver that data to high-speed disk arrays. As a Windows XP workstation, the system also lets you run software for signal analysis and post-processing. The standard configuration comes with 5 Tbytes of disk storage in a RAID array.

At the heart of the RTS 2701 is Pentek's Model 7641-420 multiband transceiver, which includes two 14-bit, 125-MHz ADCs; two 16-bit, 500-MHz DACs; digital upconverters, digital downconverters; and a FPGA-installed IP core. Together, they deliver record and playback bandwidths from 8 kHz to 60 MHz and IF frequencies to 300 MHz.

SystemFlow software includes client software that offers a control panel for the virtual instruments as well as server software that incorporates all of the real-time services for recording and playback.

Price: $44,995. *Pentek, www.pentek.com.*

Test & Measurement World

MACHINE-VISION&INSPECTION

TEST REPORT

Windows-compliant driver speeds 1394 cameras

By Ann R. Thryft, Contributing Technical Editor

Although the standard Windows FireWire bus driver works well with devices such as cameras and hard drives equipped with the IEEE 1394a interface, the driver has not been updated to take advantage of newer functions, especially higher data speeds, introduced with IEEE 1394b. Jens Hashagen, software product manager for Allied Vision Technologies, commented on how this affects engineers designing 1394b-compliant machine-vision systems running Windows, and he discussed the pros and cons of alternative 1394b bus drivers.

Q: What are the speed limitations that the original Microsoft FireWire bus driver places on 1394b-equipped cameras and other devices used in machine vision?

A: The native OHCI 1394 bus driver for Microsoft Windows XP, which was included in Microsoft's SP2 (Service Pack 2) release, was designed to operate primarily with 1394a-compatible devices. If you connect a 1394a camera to a 1394b bus using this driver, the maximum data-transfer rate on the bus decreases to 100 Mbps. The same is true if you connect a 1394b device. So, even though the 1394a maximum speed is specified at 400 Mbps, you need to do some tricks to reach that speed on a 1394b bus. And 400 Mbps is the maximum transfer rate you can reach with this driver, even for devices with a 1394b interface.

Q: How have designers of machine-vision systems coped with this situation?

A: The original 1394 driver of Windows XP SP1 (Service Pack 1) allowed 800-Mbps data-transfer rates, so for XP systems, you can run 1394b cameras at that speed. However, there is no such option if you're running Windows Vista.

The only other alternative is to use a proprietary bus driver from a camera vendor if it supports 800-Mbps data-transfer rates, as most of these drivers do, since that's why they were written. But most of these drivers are also noncompliant with the Windows 1394 standard driver. This means that other FireWire devices connected to the PC, such as hard drives, may not operate correctly.

Q: What other issues associated with the original 1394 driver affect industrial imaging?

A: There are stability issues that are unacceptable for industrial applications with high reliability demands. For example, with the Microsoft 1394 driver, an invalid packet sent in asynchronous mode could lead to an interruption of the communication between the PC and the camera, which could cause problems such as corrupt data. There's no mechanism in place to prevent that; you would have to restart the system.

Jens Hashagen
Software Product Manager
Allied Vision Technologies

Q: What has Allied Vision Technologies done to help improve this situation?

A: Besides fault-tolerant operation and low CPU load, the speed limit is the main reason we developed the AVT 1394 bus driver package. Since the driver conforms fully to the IEEE 1394 standard and complies with Microsoft's OHCI 1394 bus driver, it works with 32-bit versions of Windows, including Vista, XP, and 2000. It lets our 1394b-compliant AVT cameras transfer image data at 800 Mbps. Our bus driver can be used with the CMU (Carnegie Mellon University) 1394 camera driver, and with 1394 camera drivers based on the Microsoft bus driver, which are provided in imaging software from A&B Software, Cognex, Matrox, and National Instruments. □

INSIDE THIS REPORT

EDITOR'S NOTE

Solar, HDI light up inspection

By Ann R. Thryft, Contributing Technical Editor

Two bright spots in machine vision these days are the rise of solar-cell inspection, and the inspection of HDI (high-density interconnect) boards and their complex component packages.

As was evident at the Vision Show in Phoenix (March 31 to April 2), solar-cell manufacturers need machine vision in both front-end and back-end processes. And to produce higher volumes, drive down product costs, and increase yields, makers of photovoltaic solar cells based on silicon wafers are turning to the high-speed, high-volume manufacturing and inspection the semiconductor industry is known for, leveraging technologies and processes originally developed for semiconductors (p. 49).

Although the general economy is beginning to show signs of picking up, the machine-vision industry is still undergoing trying times, as indicated by shakeups among some manufacturers of AOI (automated optical inspection) and AXI (automated x-ray inspection) equipment. But as board interconnect and IC packages get denser and more features like passives are embedded in substrates, OEM and EMS customers need x-ray technology to see inside and under these complex structures. 3-D technology is becoming more important for electronic inspection to ensure that solder balls in ball-grid array components are shaped correctly, which can't be determined using 2-D techniques (p. 50). □

Contact Ann R. Thryft at ann@tmworld.com.

HIGHLIGHTS

System combines 3-D measurement with 2-D AOI

In addition to offering full 2-D AOI (automated optical inspection), the Zenith system from Koh Young Technology leverages 3-D inspection technology to sense and measure the z-axis profilometry of entire printed-circuit board surfaces, including electronic components, solder joints, patterns, holes, and even components with foreign materials on them. Koh Young says that unlike conventional 2-D AOI systems, the Zenith has no problem measuring dark components, lifted leads, or mislocated devices. www.kohyoung.com.

Area-scan camera family adds color models

Joining Dalsa's Falcon family of area-scan cameras are two color models that can deliver a 4-Mpixel resolution at rates of up to 60 fps. The Falcon 4M30 and 4M60 cameras also incorporate a global shutter, which eliminates such imaging issues as smearing and time-displacement artifacts.

Both the 4M30 and 4M60 provide individual color gain and offset to allow for white balancing of the image. They are programmable through a Camera Link interface and can transmit data at up to 320 MHz over distances of up to 10 m. Other features include vertical windowing, flat-field correction, exposure control, and adjustable integration time and frame rate. www.dalsa.com.

Line-scan system acquires 45,000 lines/s

The In-Sight 5604 vision system from Cognex is a high-speed line-scan imager that eliminates the need for separate PC-based software and a line-scan camera head. The self-contained unit can acquire 45,000 lines/s, which translates into 22 fps for full-sized images. It creates images with a resolution of 2 Mpixels using a 1024-pixel-wide imager and up to 2048 lines. The In-Sight 5604 employs a 1-GHz digital signal processor and includes a 10/100BaseT Ethernet port to provide connectivity to the automation control system. www.cognex.com.

AIA updates GigE Vision standard

The AIA (Automated Imaging Association) has released an updated version of the GigE Vision camera interface standard and has made the new version available in both English and Japanese. The AIA says that in addition to providing clarifications and improved documentation, Version 1.1 includes new pixel formats and Bayer format support, improved error handling, support for multiple versions of the European Machine Vision Association's GenICam programming interface, and new commands that allow action commands to be sent to multiple devices simultaneously.

In a prepared statement, Eric Carey, chair of the GigE Vision standard committee, said, "This is the first revision of the specification since it was introduced. While not introducing new camera features...the subtle changes allow developers and camera manufacturers to better control internal processes, thus allowing for more full-feature camera options."

The GigE Vision camera interface is based on the Gigabit Ethernet communications protocol. It permits data to be transferred at 1000 Mbps over cable lengths of up to 100 m. The GigE Vision standard committee is already preparing for incorporation of 10GigE as it becomes the mainstream protocol. www.machinevisiononline.org.

Machine vision aids solar-cell inspection

By Ann R. Thryft, Contributing Technical Editor

As manufacturers of solar cells face pressure to drive down costs, they are turning to higher-volume automated manufacturing, accompanied by high-speed inspection to increase yields and improve the quality of their products.

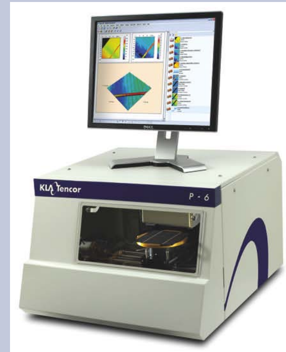
Inspection of photovoltaic solar wafers and cells is required throughout the solar-cell production process. For example, KLA-Tencor equipment inspects at several steps in the solar-cell production line, from incoming wafers to finished cells, said Jeff Donnelly, group VP of the growth and emerging markets group for KLA-Tencor. "We examine incoming bare wafers to determine their dimensions and inspect them for various defects, such as stains and microcracks," he said. "We also conduct in-line cell inspection at different process steps for excursion monitoring and to enable immediate interventions in case there are production problems, such as a defective print screen. Finally, our systems are used in the cell classifiers for final sorting and binning of completed cells."

Low dark current, low noise, and higher dynamic range enable large-array area-scan cameras such as the Pantera 22-Mpixel camera to capture a single solar cell in one shot. Courtesy of Dalsa.

The two basic kinds of photovoltaic solar-cell technologies are crystalline silicon and thin-film photovoltaic. About 86% of the industry's photovoltaic solar-cell capacity is based on crystalline silicon, in either polycrystalline or monocrystalline forms, said Donnelly. "This technology creates solar cells on top of silicon substrates, not unlike a semiconductor manufacturing process," he said. The finished active devices are then placed in a panel.

Efficiencies of silicon-based photovoltaic solar cells, typically 15 to 20% for polycrystalline and 18 to 25% for monocrystalline, are higher than efficiencies of thin-film photovoltaic cells, Donnelly said. "Developers of thin-film technologies are still using different types of substrate materials, such as plastic, glass, or very thin stainless steel, and are therefore inventing their own process equipment." Although some believe that thin film has cost advantages, KLA-Tencor has only just started to look at that technology because volumes have been so low, he said.

By leveraging industry knowledge and the technology for dealing with silicon, manufacturers can produce photovoltaic solar cells in high volumes with automated manufacturing and handling equipment. For example, KLA-Tencor's P-6 stylus surface profiler is commonly used offline in surface topology measurements, including measurements of solar cells. In March, the company's ICOS division debuted the PVI-6 system, which performs in-line optical inspection of photovoltaic solar wafers and cells, said Donnelly. The PVI-6 is a family of inspection modules combined with software, including analytical tools that increase the overall yield of the solar-cell production process.



The P-6 stylus surface profiler can be used offline in surface topology measurements, such as solar-cell metrology. Courtesy of KLA-Tencor.

Since polycrystalline solar cells are semiconductor devices, they have inspection and metrology requirements similar to those of non-solar semiconductors, and the basic inspection technologies are similar, said Donnelly. In both, the challenge is to combine high resolution with high throughput. "Typical semiconductor manufacturing throughput is 100 to 200 wafers per hour, but in solar cells, it's 2000 to 3000 wafers per hour," he said. "On the other hand, the typical scale of semiconductor inspection is in nanometers to microns, whereas for solar inspection it's in microns to millimeters. In both cases, the data sets are huge and require fairly sophisticated data processing."

In general, the solar-cell industry is moving from the research stage into the production stage, and aiming at lower costs and maximized yields, said Dave Cochrane, Dalsa's director of product management. "The market is tending toward larger [solar] panel sizes, produced for a lower cost, and with somewhat less power per square inch," he said.

In March, Dalsa announced its entrance into solar inspection with a new 22-Mpixel camera and the application of existing capabilities, such as its TDI (time delay integration) technology. "We are taking the standard technologies used in wafer inspection and other applications such as flat-panel display inspection, and tailoring them a little for the needs of solar-cell inspection," said Philip Colet, Dalsa's VP of sales and marketing. "Right now, the degree of customization is somewhat small, but as we learn more, that will increase. The main differences are in the areas of speed, sensitivity, and spectral response."

Since a solar panel can measure up to 2x2 m, the inspection equipment has to scan that surface very quickly to be efficient, said Colet. "For example, our area-scan Pantera 22-Mpixel camera takes fewer snapshots to look for gross surface defects because of its very large array," he said. "For higher volumes and higher speeds, our TDI line-scan camera is used for large, thin-film solar cells." □

FOR MORE INFORMATION:

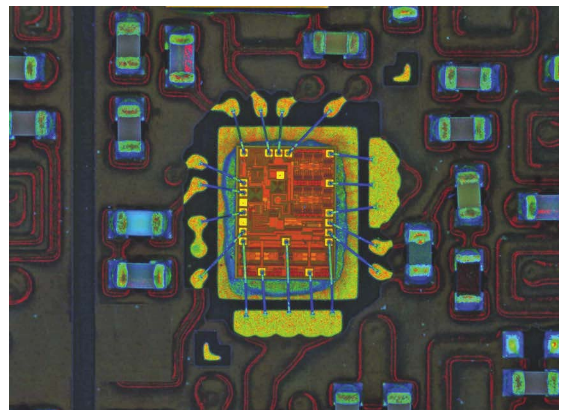
Moresco, Justin, "Solar Market: Dip in 2009, Rise by 2011," Red Herring, February 18, 2009. www.redherring.com/Home/25858.

AOI and AXI business contracts, machines improve

By Ann R. Thryft, Contributing Technical Editor

After Agilent Technologies announced in February that it would leave the AOI (automated optical inspection) and AXI (automated x-ray inspection) equipment markets, other manufacturers made related announcements. Orbotech said in its fourth quarter statement that it had signed an agreement to sell its assembled PCB (printed-circuit board) business in Europe and the Americas, but planned to continue supporting and servicing its assembled PCB installed base in the Asia-Pacific region. The company continues to make AOI equipment for bare-board PCBs, flat-panel displays, and IC substrates. Meanwhile, Machine Vision Products and Viscom each issued press releases stating that their respective AOI businesses were healthy and that each was committed to its product roadmap.

Whether Agilent's and Orbotech's actions represent the start of a wave of AOI industry contraction and consolidation remains to be seen. Omron Electronics' AOI business unit manager Chris Speck said his company hasn't seen any consolidation yet, since each equipment manufacturer has a different, proprietary technology for AOI or AXI, and they don't cross over well from one manufacturer to another. "Companies that aren't as well capitalized as others might exit the market, as well as those for whom AOI is not a key product," he said. "AOI is one of Omron's key global product lines, and we have been investing heavily in this technology."



AOI systems such as YESTech's YTV M1m inspect a board's bond wires, underfill, and surface-mount components, and look for gross die defects.
Courtesy of YESTech.

Viscom's X7056 combined AOI/AXI machine performs simultaneous optical and 3-D x-ray inspection of PCBs with dense, complex component packages like ball-grid arrays.
Courtesy of Viscom.

Other large companies might also sell off their AOI capabilities, especially if it's in a small division, said Jean-Yves Gomez, CEO of ViTechnology. "Since everyone has a different AOI technology, I don't believe there will be consolidation by technology," he said. "But there might be consolidation for the purpose of buying market share, that is, buying another company's customers."

Whether consolidation occurs will depend in part on how long a recovery takes, as well as other factors, said Carsten Salewski, CEO of Viscom. "For example, Viscom is one of the few AOI/AXI companies that is not part of a large group, [and] we are dedicated to test and inspection, most of it in electronics," he said. "As one of the market leaders, we are in a strong position, both technologically and financially, to continue with our long-term strategy." Salewski said he would expect to see more consolidation, and that "there will be fewer companies at the end of all this. The transformation of the market on the supplier side is not over yet."

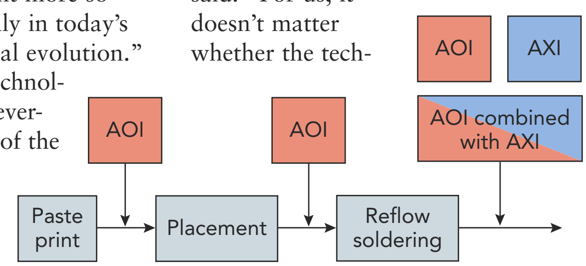
When Agilent made its announcement, the company cited commoditization in optical inspection products and the consequent lower ASPs (average selling prices), along with the large number of players, as major challenges affecting its decision. Not only is the market fragmented, but engineers use AOI technology for a variety of purposes, said Gomez. Some use AOI simply to make a "go/no-go" decision, labeling a board either OK or not OK. "They want more automation to avoid a lot of time programming, so they log known-good board information into the machine," he said.

Others use AOI to improve productivity and fine-tune production. Explained Gomez, "These customers need a high level of programmability to program parameters so they can find very small defects to improve the process. These machines are all called AOI, yet they are not the same product."

Most manufacturers agree that system prices have come down over the past few years, but they have different takes on why that has occurred. "The basis for founding YESTech in 2002 was the recognition that the inspection market and the technology—meaning, digital camera technology, and the processing power in the PC—is maturing and becoming more commoditized, and hence bringing down ASPs," said Don Miller, YESTech's CEO and president. There will still be IP (intellectual property) involved and differences among competitors, he said. "But in general, the market is offering more value and there are pricing pressures evident more so now than ever, especially in today's market. This is a natural evolution."

The key is to offer technology that addresses the ever-changing requirements of the market, said Miller. "In other words, to evolve and adapt and upgrade your product offering in response to the advancements in the technology that you are trying to inspect. This is the reason for adopting the commoditization instead of hiding from it. In this industry, if you are locked into IP from even just five years ago, you're not moving fast enough to keep up. For customers, the benefit is they are getting more capability for a lower price, and a quicker return on investment."

Salewski said it's important to differentiate between lower-end image-comparison AOI systems versus higher-end algorithm-based AOI systems. The first type "learn" from known-good samples and traditionally are simpler to program. But over time, it becomes less easy to change the program because the database of known-good samples originating in normal process variations continues to increase. In addition, since there's a greater variation of good images, the probability of missing real defects becomes higher.



Although some EMS companies only use AXI at the end of the line to catch defects that AOI has not detected, combining both functions in one machine can be more cost-effective, since the per-component cost for x-ray inspection is usually higher than the same for optical inspection. Courtesy of Viscom.

The second type of AOI system consists of high-end machines commonly used for a zero-defect strategy in medical, military, automotive, and industrial applications, and consequently, they require more sophisticated programming. "Algorithm-based AOI systems are perceived as requiring a longer learning curve to program and operate," said Salewski. "But the long-term results are that you always know not just whether an item has been classified good or bad, but why." At the high end, Viscom looks at the cost of its product and reduces it where possible, "but we don't compromise on the results," he said. "For us, it doesn't matter whether the technology used is optical or x-ray because we combine them. In our combined AOI/AXI approach, we have been very price sensitive."

Not everyone in the industry agrees that products are becoming more commoditized. "I don't think AOI equipment is becoming a commodity product, since it's much too high tech," said Speck of Omron. "Companies are not manufacturing these products any cheaper than they were a year or two ago. However, the ASPs of the base equipment have clearly come down as a result of AOI companies attempting to gain market share by reducing their profit margins."

"We do not feel a $100,000 [US] AOI system is a commodity, much less a $500,000 x-ray machine," said Jim Lin, VP of sales and marketing for TRI. "These are major investments by our customers and we treat them as such. However, TRI is a Taiwanese company, and we have always been very close to Taiwanese OEM and EMS [electronics manufacturing service] companies, which are very cost-conscious."

These customers were looking for alternatives to the premium prices that some other AOI manufacturers were charging. Therefore, Lin said, TRI's business model from the beginning was to be very cost-effective. "ASPs do come down on the same model, perhaps 5% per year. But we get that back by introducing new models with more advanced features. From the customer's point of view, they keep paying the same price and get better value."

AOI is becoming very commoditized only for those who want a go/no-go machine, where there's a lot of price pressure and competition on specifications, said Gomez. But other customers want to improve their processes, fine-tune parameters, understand what's wrong in the production line, and get warnings when a process has drifted so they can react before a process's limits are reached. "To meet these customers' needs, give them higher ROI [return on investment], and create added value," said Gomez, "vendors need to continually create new hardware and new algorithms, so these vendors suffer somewhat less from price pressure."

Omron's VT-S700 in-line AOI system is designed to improve soldered component inspection accuracy and increase throughput by shortening tact time with an expanded field of view. Courtesy of Omron.

Several manufacturers agree that, given the current business climate, it's likely more vendors will leave the business and some consolidation may occur. Others, such as Viscom's Salewski, believe that some recovery in the PCB assembly business could come as early as next year. "Meanwhile, if a smaller EMS goes out of business, there will likely be products that must be produced anyway, so that piece of business may get picked up by someone else," he said.

AOI and AXI machines continue to improve, driven in part by changes in the technologies they inspect. Gomez said that 3-D is becoming important in AOI for both semiconductor and PCB inspection. "With BGA [ball-grid array] components, you need to be sure that all solder balls have the right shape for correct solder reflow, and 3-D inspection can give good information on that shape."

Salewski added that interfacing with SPC (statistical process control), which is enabled by software, is a growing requirement.

"Agilent was the king of x-ray inspection technology, and now that

AOI systems such as ViTechnology's 5K series are increasingly interfacing with SPC software. Courtesy of ViTechnology.

In-line AXI systems like TRI's TR7600 use x-ray technology to penetrate PCBs and components and capture test images, during pre- and post-reflow. Courtesy of TRI.

they have left the market, it's not clear where this technology is headed," said Lin of TRI. "X-ray technology is pushed forward by customer requirements, such as the increase in dense IC packages like system-in-package, ball-grid array, and quad flat pack."

Lin said that, in the future, high-density interconnect boards and embedded passive components will become more popular, and equipment manufacturers will have to adjust to these new technologies. "3-D in-line x-ray inspection systems will be a big part of the answer to these challenges for our customers in the data communications, telecommunications, and automotive industries." □

FOR MORE INFORMATION:

"Agilent Exits AOI and AXI Business—Frequently Asked Questions," www.agilent.com/find/inspection.

"MachineVision Products, Inc., Celebrates its 15th Year of Continuous Service to the AOI Industry," www.visionpro.com/website/MVP_News.html#anan021409.

"Orbotech Announces Fourth Quarter and Full Year Results for 2008," www.orbotech.com/Eng/D3_Article/MenuId/527/Id/98/.

"Viscom concentrates its focus on 2-D and 3-D AOI, SPI and AXI," www.viscom.com/en/pm_view.php?cc=enus&press_id=145&pid=

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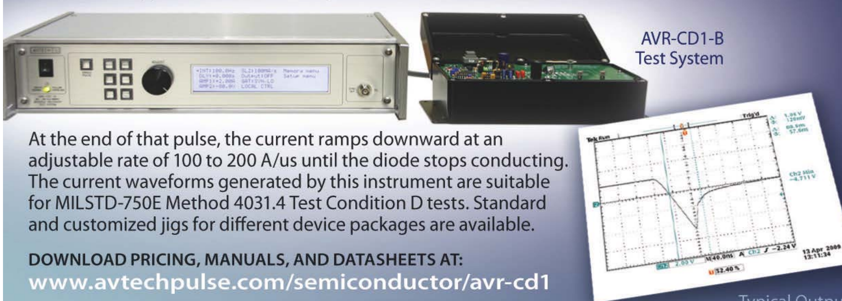

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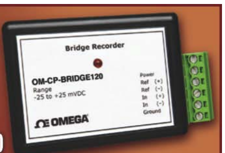

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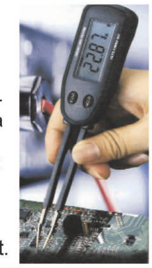

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VIEWPOINT

[An exclusive interview with a technical leader]

RICHARD HOUSE
VP, Operations-ATE
VI Technology
Austin, TX

Richard House has more than 20 years of experience in engineering, marketing, and corporate operations in the test and measurement field. In March, following the acquisition of VI Technology by Aeroflex, House became VP of operations-ATE. Prior to the acquisition, he had been at VI for 10 years and served as the company's president since 2002. Before joining VI, House spent 11 years with National Instruments, where he held the positions of director of engineering and strategic marketing manager. He holds a BS degree in electrical and computer engineering from the University of Texas.

Contributing editor Larry Maloney conducted a phone interview with House on the role of engineering services and test-management software in curbing test costs.

Tools to tackle costs and complexity

Q: What is the biggest challenge facing your test engineer customers?

A: Costs, particularly cost per unit tested during production. Companies are often willing to pay more for test systems that will test more units faster. So, there is more pressure to select the right hardware and software for test, as well as to more effectively manage test plans and test data.

At the same time, companies want to accomplish more with fewer test engineers. Sometimes that leads to a situation where much of the knowledge about a test setup is in the head of a single engineer. Meanwhile, the number and complexity of tests continue to grow as manufacturers add more features to products like smart phones. You aren't just testing a telephone; you're testing a GPS system, a video player, an MP3 player, and a camera.

Q: How does VI's Arendar platform address these challenges?

A: The complexity of today's products leads to more testing at all stages—R&D, production, and field maintenance. Different versions of a product also typically require changes in test hardware, software, and calibration. You have a barrage of test data that managers and engineers must track, compare, and analyze. If you do a poor job of managing this data, you get wasted time, higher costs, and even poor product quality.

Our Arendar software creates a system for managing the test data generated from the very start of product development. In addition, our newest version—Arendar 2009—includes a new test-plan module that models all the information required to perform tests. From your Web browser, you can control test order, pass/fail limits, parameters, hardware configuration, and test-sequencing software. You can also deploy test code into test stations, monitor test-plan execution, view comments from engineering staff, and create real-time test reports.

Q: How did VI come to develop its new Multimedia Test System (MMTS)?

A: It is an outgrowth of our enterprise test business, which serves companies that do not want to use internal resources to design ATE (automatic test equipment) systems for the complex products we've been talking about. They would rather have their engineers focus on product development than to have them take time out to devise needed tests—particularly at the production stage.

The MMTS, which this year won a Best in Test award from your magazine, includes all the hardware, software, and fixtures needed for testing analog and digital audio and video, power sources, USB, modem, and Ethernet connectivity. In most cases, the MMTS is deployed in production, where it can test four devices simultaneously. It can also be configured in many different versions, depending on the device being tested.

Q: What synergies do you see between VI Technology and your new parent, Aeroflex?

A: Aeroflex is very strong in high-frequency RF and broadband test systems, while VI has a lot of experience in baseband test. This gives Aeroflex customers a broader range of solutions. Being part of the much larger Aeroflex also gives VI added credibility as we seek to provide customers with test systems that can be replicated throughout their enterprises. It also accelerates VI's ability to expand globally, and although our ideas must compete with those of other Aeroflex operations, we will have the opportunity for added financial resources to develop new platforms like the MMTS. T&MW

Richard House answers more questions on test-data management and targeted test solutions in the online version of this interview: www.tmworld.com/2009_06.